Design Example Report

Title	***High efficiency 180 W USB Power Supply using InnoSwitch™5-Pro with 900 V PowiGaN (INN5496F) and HiperPFS™-5 (PFS5278F)***
Specification	USB PD 3.1 EPR charger delivering up to 36 V
Application	Rapid charging for Notebooks and Power Tools
Author	Applications Engineering Department
Document Number	DER-1046
Date	October 24, 2024
Revision	A

Summary and Features

- High Efficiency across line and load
  - 93.4% at 90 VAC, 93.9% at 115 VAC (36 V / 5 A load)94.5% at 230 VAC, 94.6% at 265 VAC (36 V / 5 A load)
  - PowiGaN™ PFC and flyback power switches
  - Semi-active bridge rectifier increases efficiency by up to 0.7%
- Less than 70 mW no-load consumption at 230 VAC
  - Active discharge of X capacitor in EMI filter by HiperPFS-5 IC reduces no-load consumption
- PFC stage with HiperPFS-5
  - DCM mode boost PFC with small boost inductor and standard recovery boost diode
- DC-DC Flyback with Synchronous Rectification Zero Voltage Switching (SR-ZVS)

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- Ensures very low turn-on losses of the primary switch without the need for an active-clamp circuit
-

- Supports the following PDOs
  - SPR Fixed PDO 5 V 3 A
  - SPR Fixed PDO 9 V 3 A
  - SPR Fixed PDO 12 V 3 A
  - SPR Fixed PDO 15 V 3 A
  - SPR Fixed PDO 20 V 5 A
  - EPR Fixed PDO 28 V 5 A
  - EPR Fixed PDO 36 V 5 A
  - EPR AVS PDO 15 V-36 5 A

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PATENT INFORMATION
The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

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1 Schematic

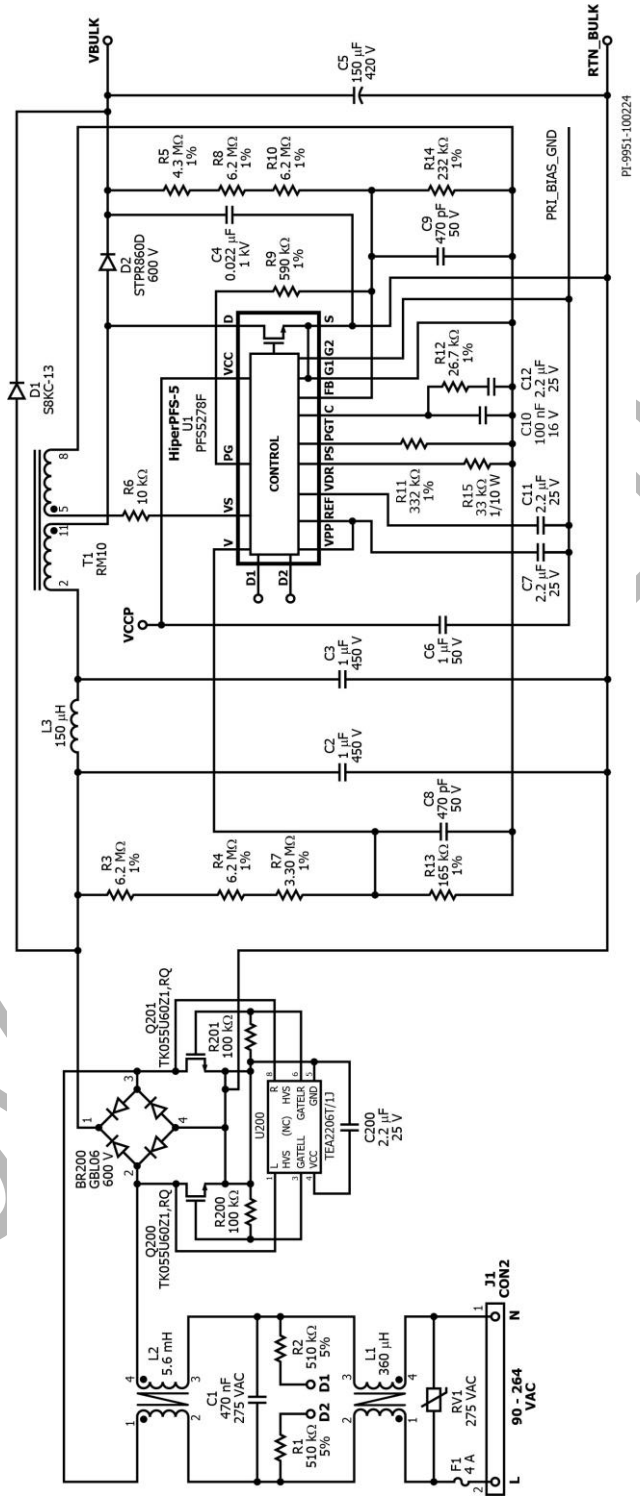

Figure 1 – Input Stage and PFC Schematic

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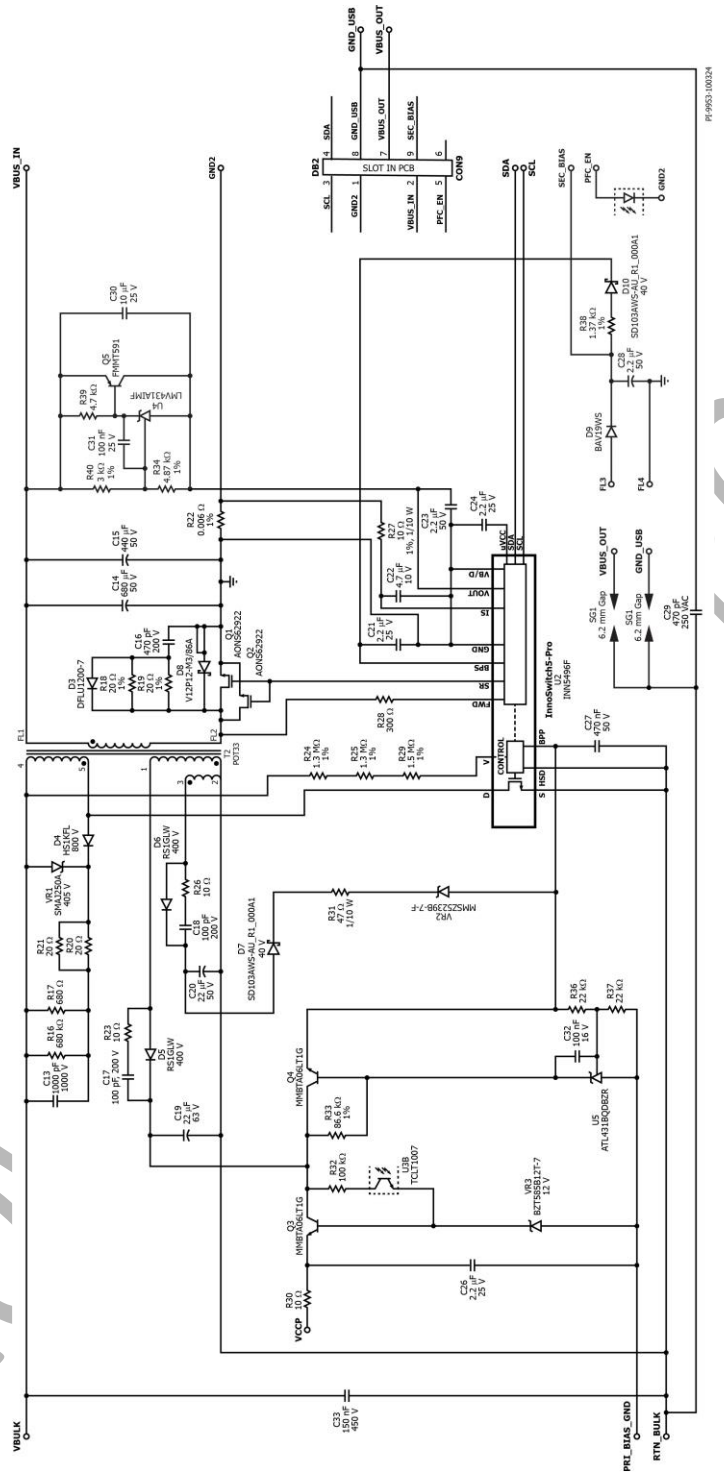

Figure 2 – Flyback Section Schematic

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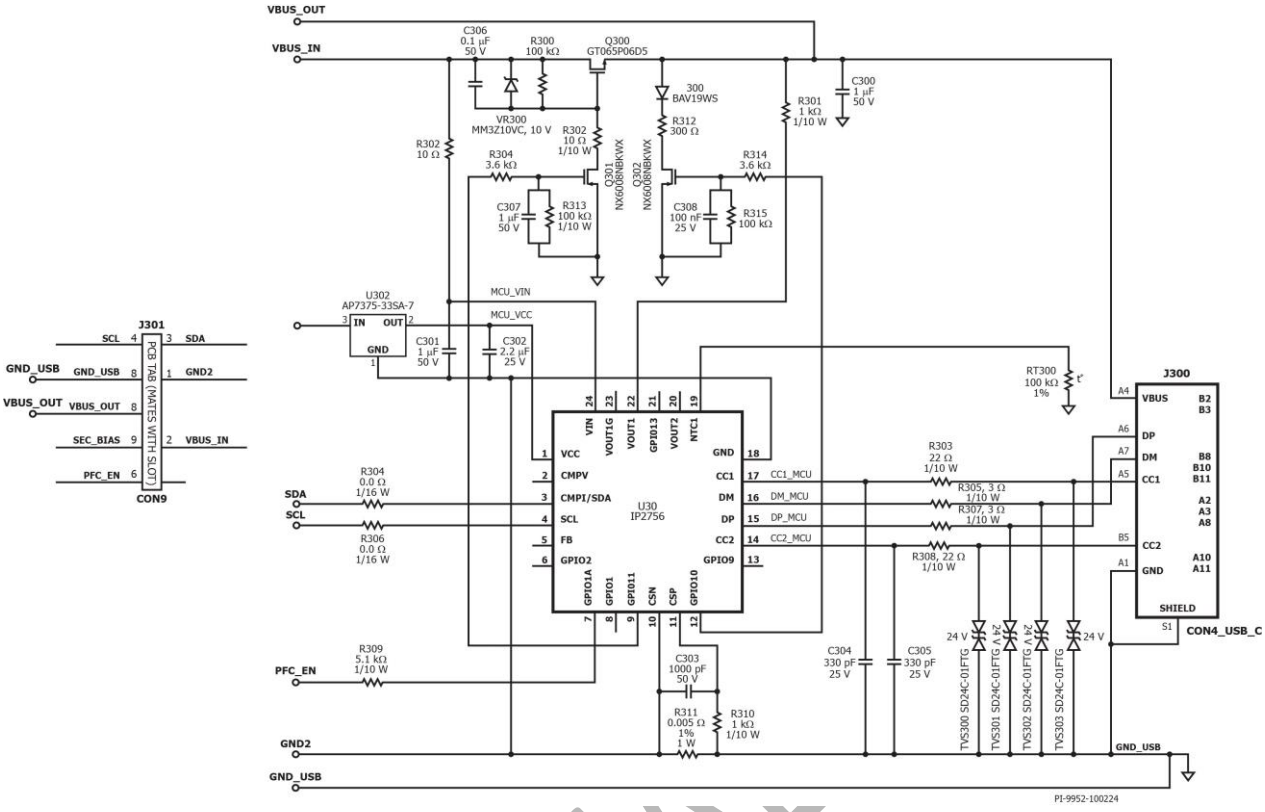

Figure 3 – USB-PD Daughter Board Schematic

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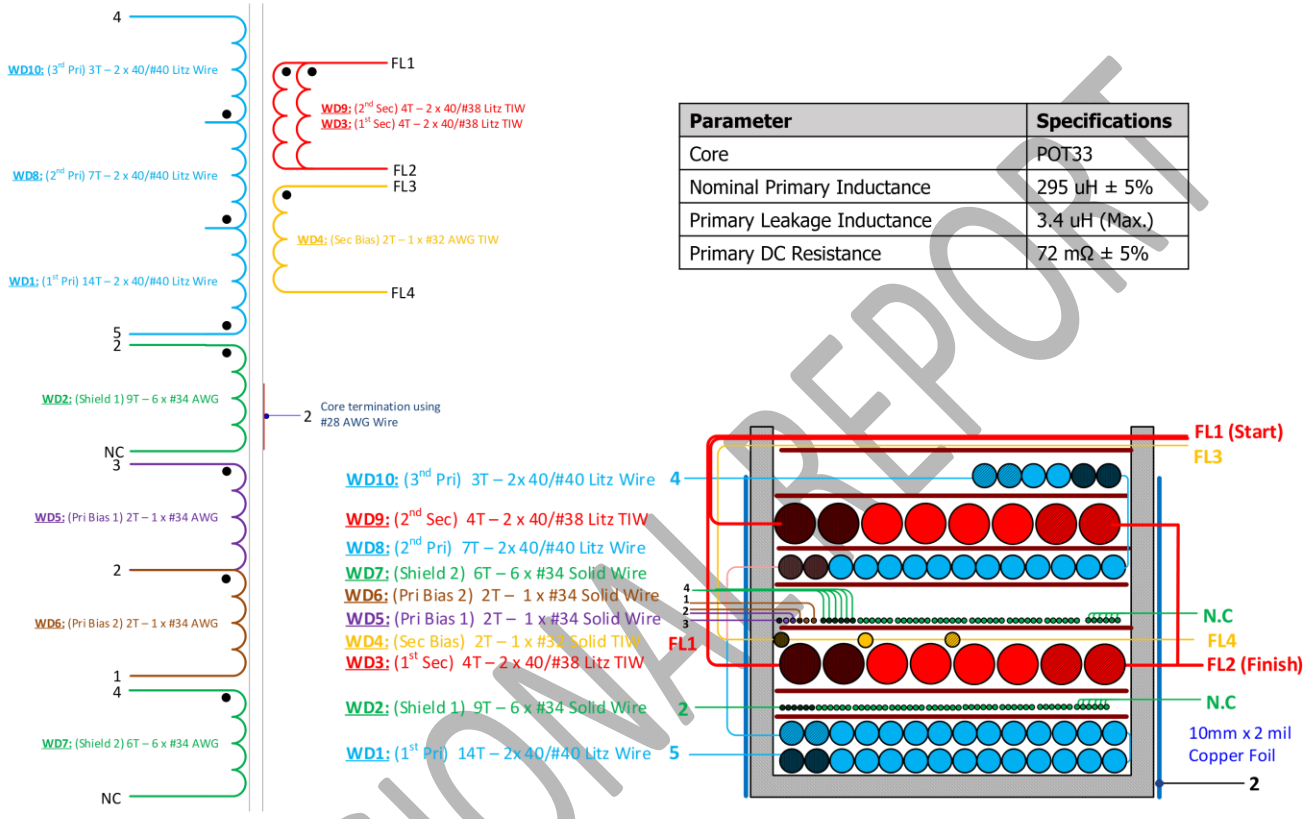
2 Transformer Build Diagram

2.1 Flyback Transformer



Parameter	Specifications
Core	POT33
Nominal Primary Inductance	295 uH ± 5%
Primary Leakage Inductance	3.4 uH (Max.)
Primary DC Resistance	72 mΩ ± 5%

Figure 4 – Flyback Transformer Diagram

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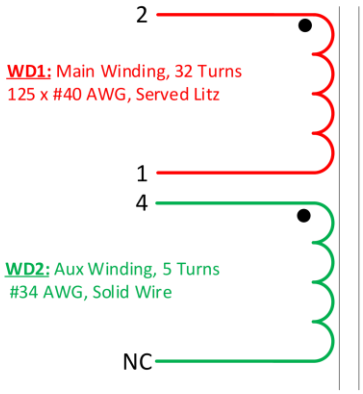
2.2 Power Factor Corrector Choke



Parameter	Specifications
Core	RM10
Nominal Primary Inductance	134 uH ± 5%
Primary DC Resistance	55 mΩ ± 5%

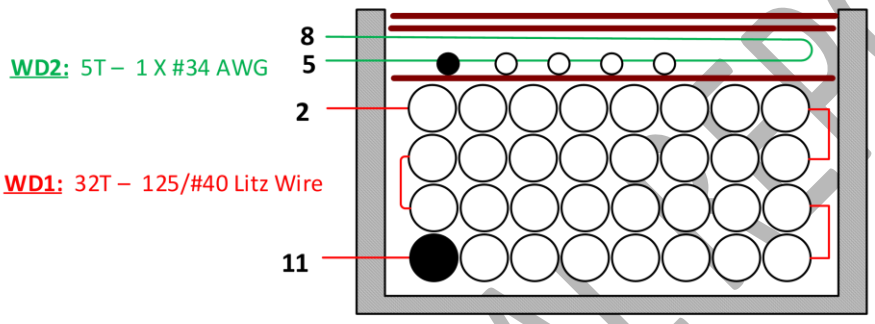


Figure 5 – Power Factor Corrector Choke Diagram

3 Performance Data

3.1 No-Load Input Power

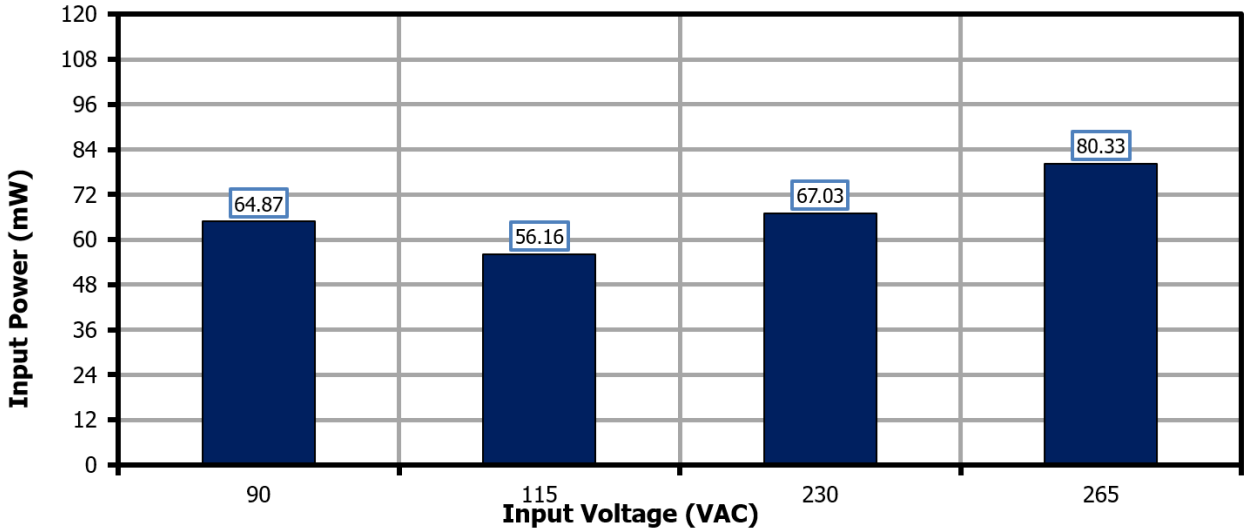


Figure 6 – No-Load Input Power

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Note: The PD controller was disconnected for no-load measurements.

3.2 Efficiency

3.2.1 36 V Output

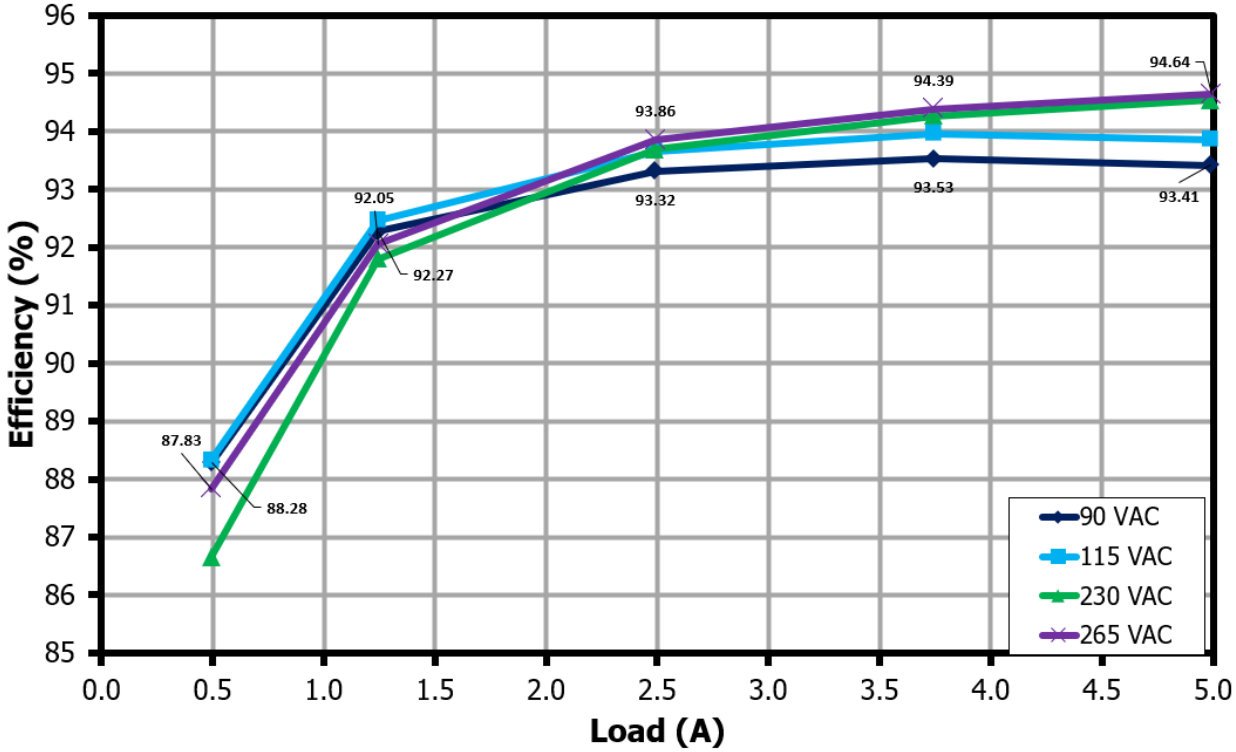

Figure 7 – 36 V Output

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3.2.2 28 V Output

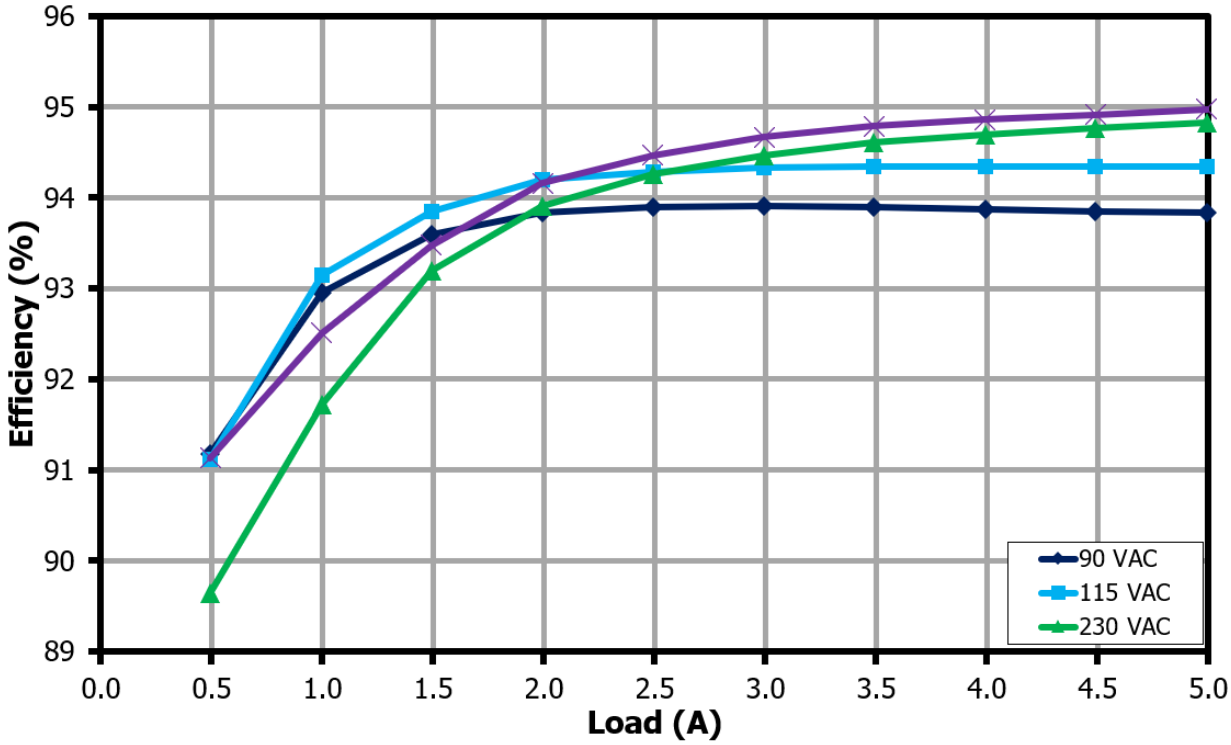

Figure 8 – 28 V Output

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3.2.3 20 V Output

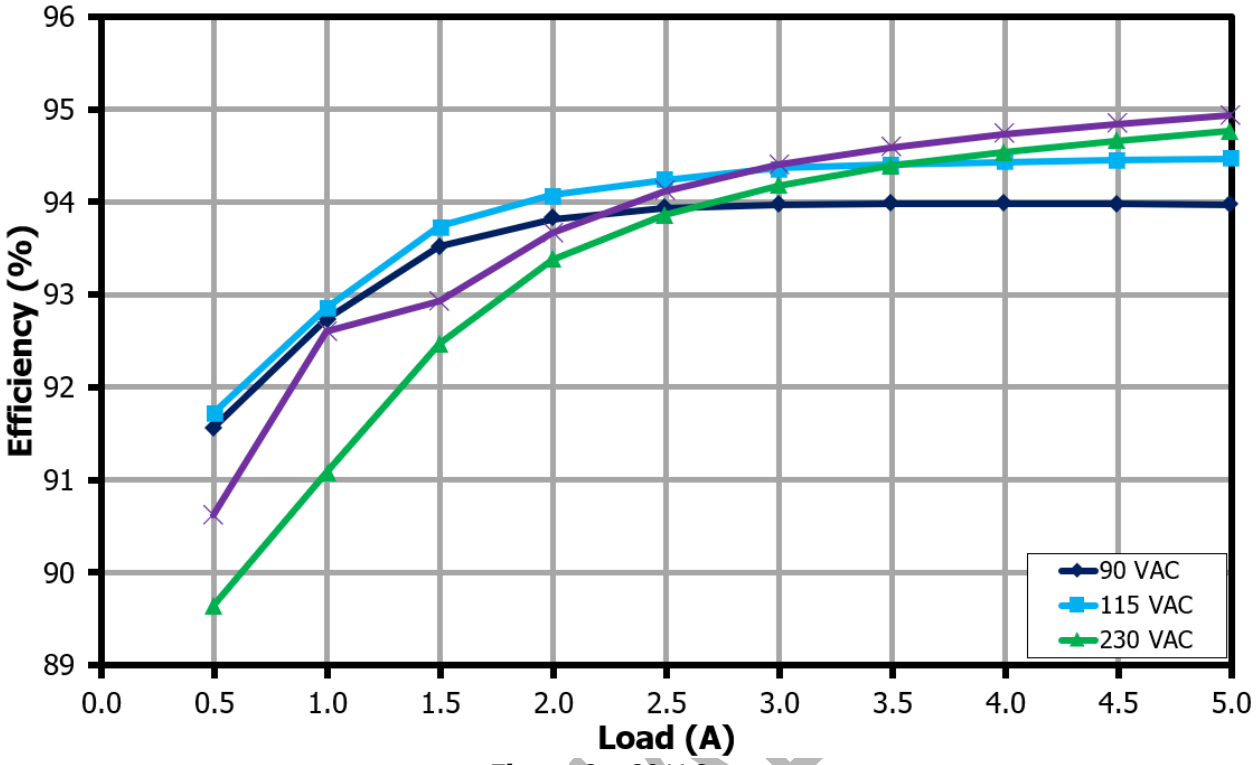

Figure 9 – 20 V Output

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4 Revision History

Date	Author	Revision	Description & Changes	Reviewed
10/24/2024	Applications	A	First release (Provisional)	Apps & Mktg

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