International
IOR Rectifier

Preliminary Datasheet 12/20/2011

IRMCF143

High Performance Sensorless Motor Control IC

Features

- **MCE™ (Flexible Motion Control Engine) - Dedicated computation engine for high efficiency sinusoidal sensorless motor control**
- **Built-in hardware peripheral for single shunt current feedback reconstruction and analog circuits**
- **Supports induction machine and both interior and surface permanent magnet motor sensorless control**
- **Dedicated PFC PWM for digital PFC control**
- **Loss minimization Space Vector PWM**
- **Two-channel analog output (PWM)**
- **Embedded 8-bit high speed microcontroller (8051) for flexible I/O and man-machine control**
- **JTAG programming port for emulation/debugger**
- **Serial communication interface (UART)**
- **I^2C/SPI serial interface**
- **Three general purpose timers/counters**
- **Two special timers: periodic timer, capture timer**
- **Watchdog timer with independent internal clock**
- **Internal 64 Kbyte flash memory**
- **5V tolerant I/O**
- **3.3V single supply**

Product Summary

Maximum clock input ($f_{crystal}$)	60 MHz
Maximum Internal clock (SYSCLK)	120MHz
Maximum 8051 clock (8051CLK)	20MHz
Sensorless control computation time	35 µsec@100MHz
MCE™ computation data range	16 bit signed
8051 Program Flash	52KB
805/MCE Data RAM	4KB
MCE Program RAM	12KB
GateKill latency (digital filtered)	2 µsec
PWM carrier frequency	20 bits/ SYSCLK
A/D input channels	8
A/D converter resolution	12 bits
A/D converter conversion speed	2 µsec
Analog output (PWM) resolution	8 bits
UART baud rate (typ)	57.6K bps
Number of I/O (max)	21
Package (lead free)	QFP64

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Description

IRMCF143 is a high performance Flash based motion control IC designed primarily for appliance applications. IRMCF143 is designed to achieve low cost yet high performance control solutions for advanced inverterized appliance motor control. IRMCF143 contains two computation engines. One is the Flexible Motion Control Engine (MCE™) for sensorless control of permanent magnet motors or induction motors; the other is an 8-bit high-speed microcontroller (8051). Both computation engines are integrated into one monolithic chip. The MCE™ contains a collection of control elements implemented in a dedicated computation engine such as Proportional plus Integral, Vector rotator, Angle estimator, Multiply/Divide, Low loss SVPWM and Single Shunt IFB. The user can program a motion control algorithm by connecting these control elements using a graphic compiler. Key components of the complex sensorless control algorithms, such as the Angle Estimator, are provided as complete pre-defined control blocks. A unique analog/digital circuit and algorithm to fully support single shunt current reconstruction is also provided. The 8051 microcontroller performs 2-cycle instruction execution (10MIPS at 20MHz 8051CLK). The MCE and 8051 microcontroller are connected via dual port RAM for signal monitoring and command input. An advanced graphic compiler for the MCE™ is seamlessly integrated into the MATLAB/Simulink environment, while third party JTAG-based emulator tools are supported for 8051 software development. IRMCF143 comes in a 64 pin QFP package.

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1 Overview

IRMCF143 is a new generation International Rectifier integrated circuit device primarily designed as a one-chip solution for complete inverter controlled appliance motor control applications. Unlike a traditional microcontroller or DSP, the IRMCF143 provides a built-in closed loop sensorless control algorithm using the unique Flexible Motion Control Engine (MCE™) for permanent magnet motors as well as induction motors. The MCE™ consists of a collection of control elements, motion peripherals, a dedicated motion control sequencer and dual port RAM to map internal signal nodes. IRMCF143 also employs a unique single shunt current reconstruction circuit to eliminate additional analog/digital circuitry and enables a direct shunt resistor interface to the IC. Motion control programming is achieved using a dedicated graphical compiler integrated into the MATLAB/Simulink™ development environment. Sequencing, user interface, host communication, and upper layer control tasks can be implemented in the 8051 high-speed 8-bit microcontroller. The 8051 microcontroller is equipped with a JTAG port to facilitate emulation and debugging tools. Figure 1 shows a typical application schematic using the IRMCF143.

IRMCF143 contains 64 Kbytes of Flash program memory. The IRMCK143 contains 32 Kbytes OTP memory and is intended for high volume production purposes while the IRMCF143 is intended for flexible volume production. Both the Flash and ROM versions come in a 64-pin QFP package with identical pin configuration to facilitate PC board layout and transition to mass production.

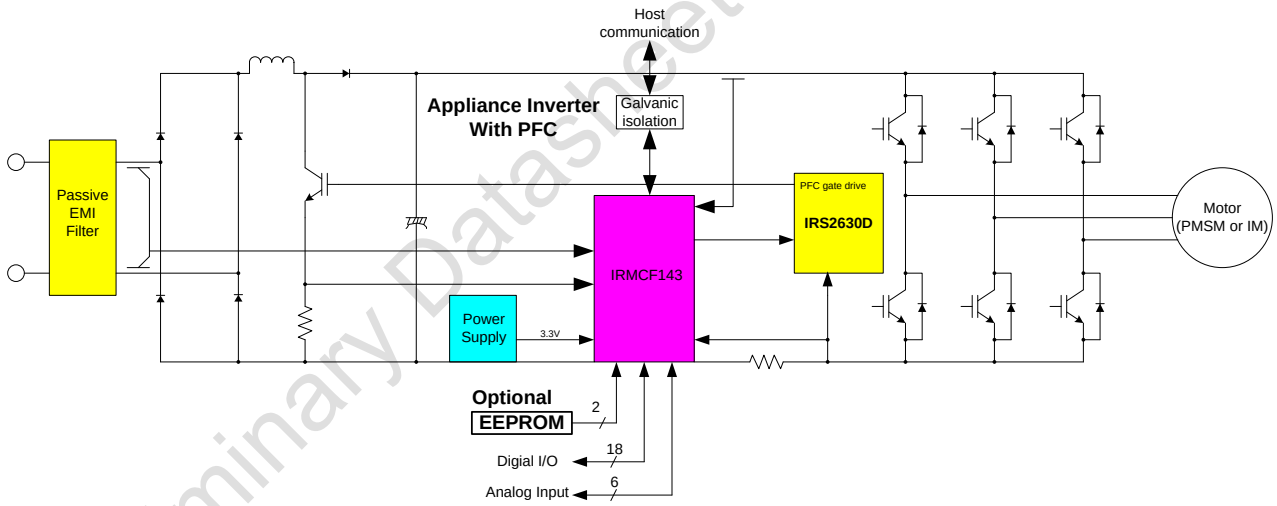

Figure 1. Typical Application Block Diagram Using IRMCF143

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2 PINOUT

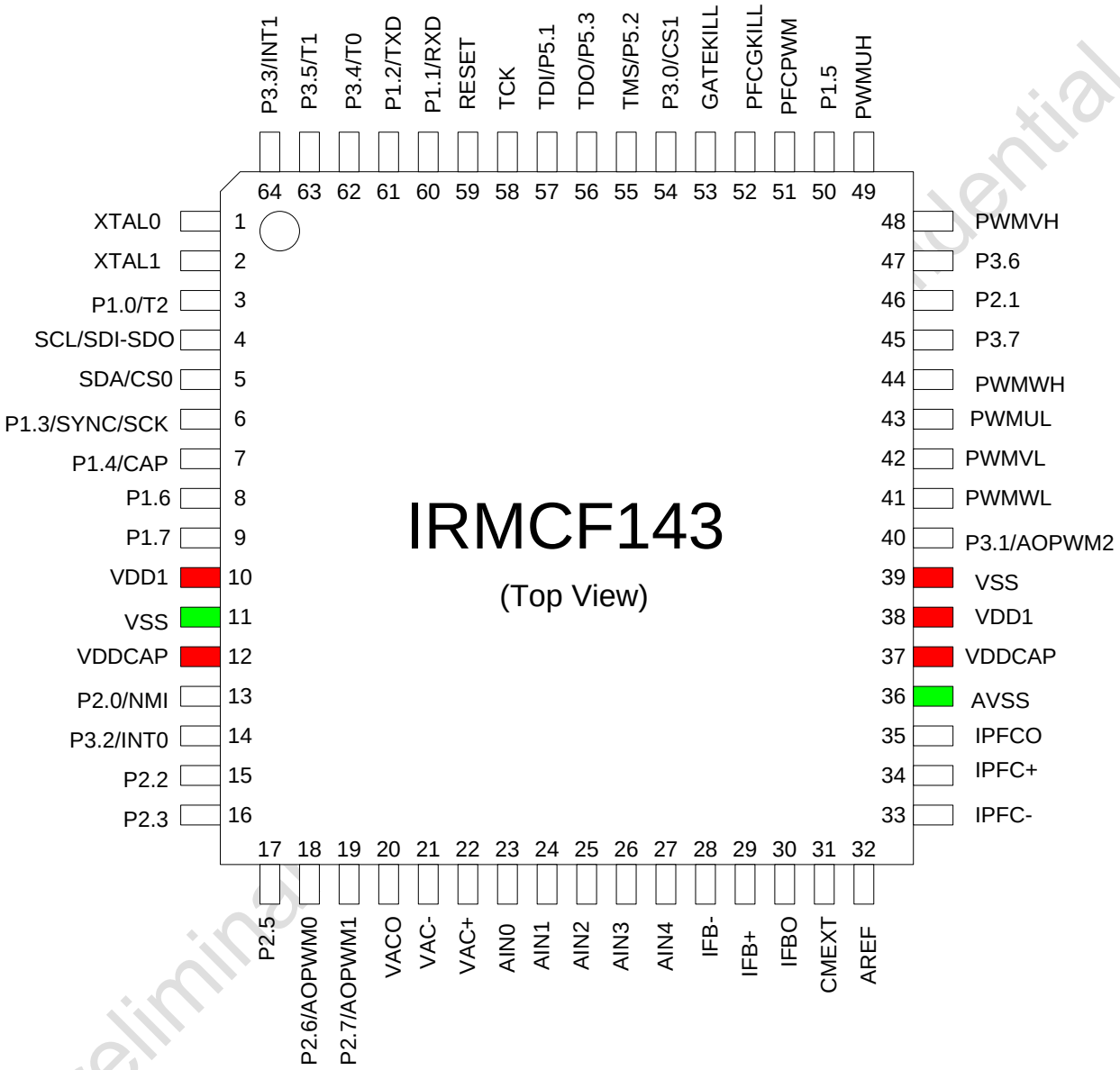

Figure 2 Pinout of IRMCF143

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3 IRMCF143 Block Diagram and Main Functions

IRMCF143 block diagram is shown in Figure 3.

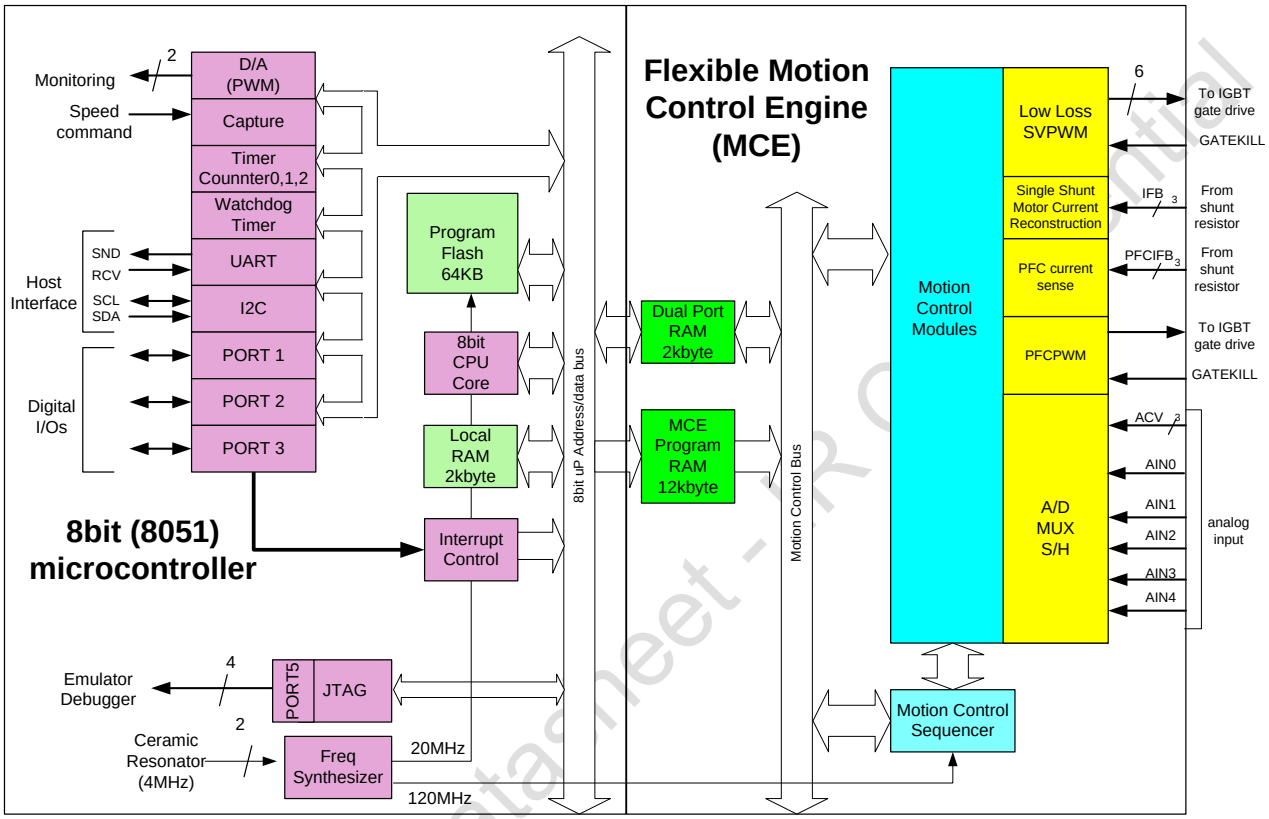

Figure 3 IRMCF143 Block Diagram

IRMCF143 contains the following functions for sensorless AC motor control applications:

- Motion Control Engine (MCE™)
  - Sensorless FOC (complete sensorless field oriented control)
  - Proportional plus Integral block
  - Low pass filter
  - Differentiator and lag (high pass filter)
  - Ramp
  - Limit
  - Angle estimate (sensorless control)
  - Inverse Clark transformation
  - Vector rotator
  - Bit latch

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- Peak detect
- Transition
- Multiply-divide (signed and unsigned)
- Divide (signed and unsigned)
- Adder
- Subtractor
- Comparator
- Counter
- Accumulator
- Switch
- Shift
- ATAN (arc tangent)
- Function block (any curve fitting, nonlinear function)
- 16 bit wide Logic operations (AND, OR, XOR, NOT, NEGATE)
- MCE™ program memory and dual port RAM (Max 12 + 2 Kbyte)
- MCE™ control sequencer

- 8051 microcontroller
  - Two 16 bit timer/counters
  - One 16 bit periodic timer
  - One 16 bit watchdog timer
  - One 16 bit capture timer
  - Up to 24 discrete I/Os
  - Eight-channel 12 bit A/D
    - Buffered (current sensing) one channel (0 – 1.2V input)
    - Unbuffered seven channels (0 – 1.2V input)
  - JTAG port (4 pins)
  - Up to three channels of analog output (8 bit PWM)
  - UART
  - I^2C/SPI port
  - 64K byte Flash memory
  - 2K byte data RAM (Configurable to change the size)

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4 Application connection and Pin function

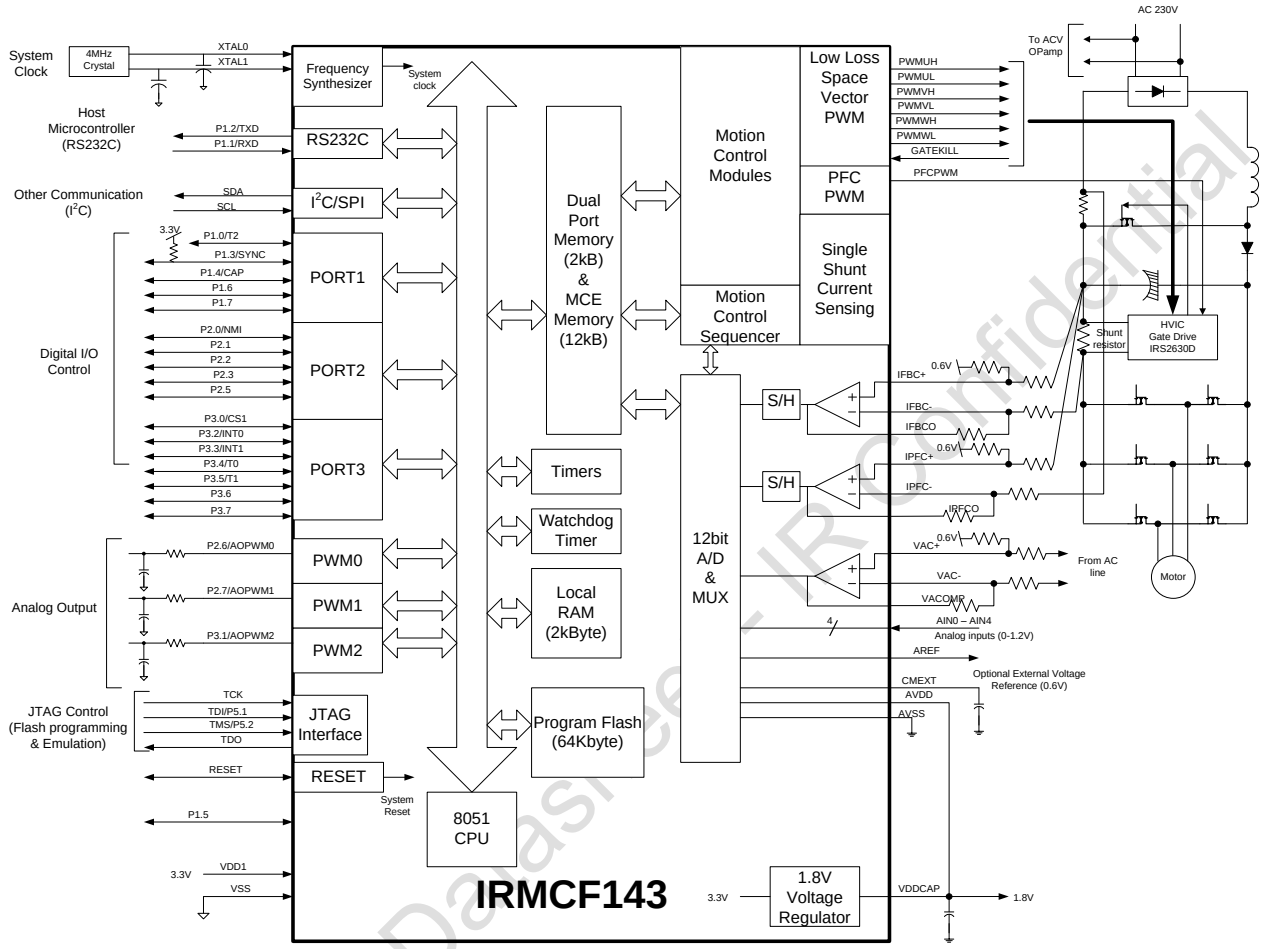

Figure 4 IRMCF143 Connection Diagram

4.1 8051 Peripheral Interface Group

UART Interface

P1.2/TXD	Output, Transmit data from IRMCF143
P1.1/RXD	Input, Receive data to IRMCF143

Discrete I/O Interface

P1.0/T2	Input/output port 1.0, can be configured as Timer/Counter 2 input
P1.1/RXD	Input/output port 1.1, can be configured as RXD input
P1.2/TXD	Input/output port 1.2, can be configured as TXD output
P1.3/SYNC/SCK	Input/output port 1.3, can be configured as SYNC output or SPI clock output
P1.4/CAP	Input/output port 1.4, can be configured as Capture Timer input
P1.5	Input/output port 1.5

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P1.6	Input/output port 1.6
P1.7	Input/output port 1.6
P2.0/NMI	Input/output port 2.0, can be configured as non-maskable interrupt input
P2.2	Input/output port 2.2
P2.3	Input/output port 2.3
P2.5	Input/output port 2.5
P2.6/AOPWM0	Input/output port 2.6, can be configured as AOPWM0 output
P2.7/AOPWM1	Input/output port 2.7, can be configured as AOPWM1 output
P3.0/INT2/CS1	Input/output port 3.0, can be configured as INT2 input or SPI chip select 1
P3.1/AOPWM2	Input/output port 3.1, can be configured as AOPWM2 output
P3.2/NINT0	Input/output port 3.2, can be configured as INT0 input
P3.3/NINT1	Input/output port 3.3, can be configured as INT1 input
P3.4/T0	Input/output port 3.4, can be configured as T0 input for counter mode
P3.5/T1	Input/output port 3.5, can be configured as T1 input for counter mode
P3.6	Input/output port 3.6
P3.7	Input/output port 3.7
P5.1/TDI	Input port, configured as JTAG port by default
P5.2/TMS	Input port, configured as JTAG port by default

Analog Output Interface

P2.6/AOPWM0	Input/output, can be configured as 8-bit PWM output 0 with programmable carrier frequency
P2.7/AOPWM1	Input/output, can be configured as 8-bit PWM output 1 with programmable carrier frequency
P3.1/AOPWM2	Input/output, can be configured as 8-bit PWM output 2 with programmable carrier frequency

Crystal Interface

XTAL0	Input, connected to crystal
XTAL1	Output, connected to crystal

Reset Interface

RESET	Input and Output, system reset, doesn't require external RC time constant

I^2C Interface

SCL/SO-SI	Output, I^2C clock output, or SPI data
SDA/CS0	Input/output, I^2C Data line or SPI chip select 0

I^2C/SPI Interface

SCL/SO-SI	Output, I^2C clock output, or SPI data
SDA/CS0	Input/output, I^2C data line or SPI chip select 0
P1.3/SYNC/SCK	Input/output port 1.3, can be configured as SYNC output or SPI clock output
P3.0/INT2/CS1	Input/output port 3.0, can be configured as INT2 input or SPI chip select 1

4.2 Motion Peripheral Interface Group

PWM

PWMUH	Output, PWM phase U high side gate signal, internally pulled down by 58kΩ, configured high true at a power up

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PWMUL	Output, PWM phase U low side gate signal, internally pulled down by 58kΩ, configured high true at a power up
PWMVH	Output, PWM phase V high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
PWMVL	Output, PWM phase V low side gate signal, internally pulled down by 58kΩ, configured high true at a power up
PWMWH	Output, PWM phase W high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
PWMWL	Output, PWM phase W low side gate signal, internally pulled down by 58kΩ, configured high true at a power up
PFCPWM	Output, PFCPWM output signal, internally pulled up by 70kΩ, configured low true at a power up

Fault

GATEKILL	Input, upon assertion, this negates all six PWM signals, programmable logic sense, internally pulled up by 70kΩ
PFCGKILL	Input, upon assertion, this negates PFCPWM signal, programmable logic sense, internally pulled up by 70kΩ

4.3 Analog Interface Group

AVSS	Analog power return, (analog internal 1.8V power is shared with VDDCAP)
AREF	0.6V buffered output
CMEXT	Unbuffered 0.6V, input to the AREF buffer, capacitor needs to be connected.
IFB+	Input, Operational amplifier positive input for shunt resistor current sensing
IFB-	Input, Operational amplifier negative input for shunt resistor current sensing
IFBO	Output, Operational amplifier output for shunt resistor current sensing
AIN0	Input, Analog input channel 0 (0 – 1.2V), typically configured for DC bus voltage input
AIN1	Input, Analog input channel 1 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN2	Input, Analog input channel 2 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN3	Input, Analog input channel 3 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN4	Input, Analog input channel 4 (0 – 1.2V), needs to be pulled down to AVSS if unused
VAC+	Input, Operational amplifier positive input for VAC channel
VAC-	Input, Operational amplifier negative input for VAC channel
VACO	Output, Operational amplifier output for VAC output, there is a single sample/hold circuit on the output
IPFC+	Input, Operational amplifier positive input for PFC current sensing channel
IPFC-	Input, Operational amplifier negative input for PFC current channel
IPFCO	Output, Operational amplifier output for PFC current sensing channel

4.4 Power Interface Group

VDD1	Digital power (3.3V)

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VDDCAP	Internal 1.8V output, requires capacitors to the pin. Shared with analog power pad internally **Note:** The internal 1.8V supply is not designed to power any external circuits or devices. Only capacitors should be connected to this pin.
VSS	Digital common

4.5 Test Interface Group

P5.2/TMS	JTAG test mode input or input digital port
TDO	JTAG data output
P5.1/TDI	JTAG data input or input digital port
TCK	JTAG test clock

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5 DC Characteristics

5.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Condition
V_{DD1}	Supply Voltage	-0.3 V	-	3.6 V	Respect to VSS
V_{IA}	Analog Input Voltage	-0.3 V	-	1.98 V	Respect to AVSS
V_{ID}	Digital Input Voltage	-0.3 V	-	6.0 V	Respect to VSS
T_A	Ambient Temperature	-40 ˚C	-	85 ˚C	
T_S	Storage Temperature	-65 ˚C	-	150 ˚C	

Table 1. Absolute Maximum Ratings

Caution: Stresses beyond those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

5.2 System Clock Frequency and Power Consumption

C_{AREF} = 1nF, C_{MEXT}= 100nF. VDD1=3.3V, Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
SYSCLK	System Clock	32	-	120	**MHz**
P_D	Power consumption		160[1)]	TBD	**mW**

Table 2. System Clock Frequency

Note 1) The value is based on the condition of MCE clock=120MHz, 8051 clock 20MHz with a actual motor running by a typical MCE application program and 8051 code.

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5.3 Digital I/O DC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
V_{DD1}	Supply Voltage	3.0 V	3.3 V	3.6 V	Recommended
V_{IL}	Input Low Voltage	-0.3 V	-	0.8 V	Recommended
V_{IH}	Input High Voltage	2.0 V		3.6 V	Recommended
C_{IN}	Input capacitance	-	3.6 pF	-	(1)
I_L	Input leakage current		±10 nA	±1 µA	V_O = 3.3 V or 0 V
I_{OL1}(2)	Low level output current	8.9 mA	13.2 mA	15.2 mA	V_{OL} = 0.4 V (1)
I_{OH1}(2)	High level output current	12.4 mA	24.8 mA	38 mA	V_{OH} = 2.4 V (1)
I_{OL2}(3)	Low level output current	17.9 mA	26.3 mA	33.4 mA	V_{OL} = 0.4 V (1)
I_{OH2}(3)	High level output current	24.6 mA	49.5 mA	81 mA	V_{OH} = 2.4 V (1)

Table 3. Digital I/O DC Characteristics

Note:
(1) Data guaranteed by design.
(2) Applied to SCL/SO-SI, SDA/CS0 pins.
(3) Applied to all digital I/O pins except SCL/SO-SI and SDA/CS0 pins.

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5.4 PLL and Oscillator DC characteristics

C_{AREF} = 1nF, C_{MEXT}= 100nF. VDD1=3.3V, Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
$V_{IL\ OSC}$	Oscillator (XTAL0,1) Input Low Voltage	0	-	0.2* V_{DDCAP}	V_{DDCAP} = voltage at VDDCAP pin
$V_{IH\ OSC}$	Oscillator (XTAL0,1) Input High Voltage	0.8* V_{DDCAP}	-	V_{DDCAP}	V_{DDCAP} = voltage at VDDCAP pin

Table 4 PLL DC Characteristics

5.5 Analog I/O DC Characteristics

- OP amp for current sensing (IFB+, IFB-, IFBO)

C_{AREF} = 1nF, C_{MEXT}= 100nF. VDD1=3.3V, Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
V_{OFFSET}	Input Offset Voltage	-	-	26 mV	V_{AVDD} = 1.8 V
V_I	Input Voltage Range	0 V		1.2 V	Recommended
V_{OUTSW}	OP amp output operating range	50 mV (1)	-	1.2 V	V_{AVDD} = 1.8 V
C_{IN}	Input capacitance	-	3.6 pF	-	(1)
R_{FDBK}	OP amp feedback resistor	5 kΩ	-	20 kΩ	Requested between IFBO and IFB-
OP_{GAINCL}	Operating Close loop Gain	80 db	-	-	(1)
CMRR	Common Mode Rejection Ratio	-	80 db	-	(1)
I_{SRC}	Op amp output source current	-	1 mA	-	V_{OUT} = 0.6 V (1)
I_{SNK}	Op amp output sink current	-	100 µA	-	V_{OUT} = 0.6 V (1)

Table 5. Analog I/O DC Characteristics

Note:
(1) Data guaranteed by design.

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5.6 Under Voltage Lockout DC characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
UV_{CC+}	UVcc positive going Threshold	2.78 V	3.04 V	3.13 V	(1)
UV_{CC-}	UVcc negative going Threshold	2.78 V	2.97 V	3.13 V	
$UV_{CC}H$	UVcc Hysteresys	-	73 mV	-	(1)

Table 6. UVcc DC Characteristics

Note:
(1) Data guaranteed by design.

5.7 Itrip comparator DC characteristics

Unless specified, VDD1=3.3V, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
$Itrip_{+}$	Itrip positive going Threshold	-	1.22V	-	V_{DD1} = 3.3 V
$Itrip_{-}$	Itrip negative going Threshold	-	1.10V	-	V_{DD1} = 3.3 V
ItripH	Itrip Hysteresys	-	120mV	-	

Table 7. Itrip DC Characteristics

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5.8 CMEXT and AREF Characteristics

C_{AREF} = 1nF, C_{MEXT}= 100nF. Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
V_{CM}	CMEXT voltage	495 mV	600 mV	700 mV	V_{AVDD} = 1.8 V
V_{AREF}	Buffer Output Voltage	495 mV	600 mV	700 mV	V_{AVDD} = 1.8 V
ΔV_o	Load regulation (V_{DC}-0.6)	-	1 mV	-	(1)
PSRR	Power Supply Rejection Ratio	-	75 db	-	(1)

Table 8. CMEXT and AREF DC Characteristics

Note:

(1) Data guaranteed by design.

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6 AC Characteristics

6.1 Digital PLL AC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
F_{CLKIN}	Crystal input frequency	3.2 MHz	4 MHz	60 MHz	(1) (see figure below)
F_{PLL}	Internal clock frequency	32 MHz	50 MHz	128 MHz	(1)
F_{LWPW}	Sleep mode output frequency	$F_{CLKIN} \div 256$	-	-	(1)
J_S	Short time jitter	-	200 psec	-	(1)
D	Duty cycle	-	50 %	-	(1)
T_{LOCK}	PLL lock time	-	-	500 µsec	(1)

Table 9. PLL AC Characteristics

Note:
(1) Data guaranteed by design.

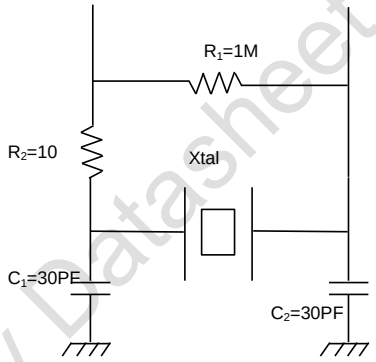

Figure 5. Crystal circuit example

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6.2 Analog to Digital Converter AC Characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
T_{CONV}	Conversion time	-	-	2.05 µsec	(1)
T_{HOLD}	Sample/Hold maximum hold time	-	-	10 µsec	Voltage droop ≤ 15 LSB (see figure below)

Table 10 . A/D Converter AC Characteristics

Note:
(1) Data guaranteed by design.

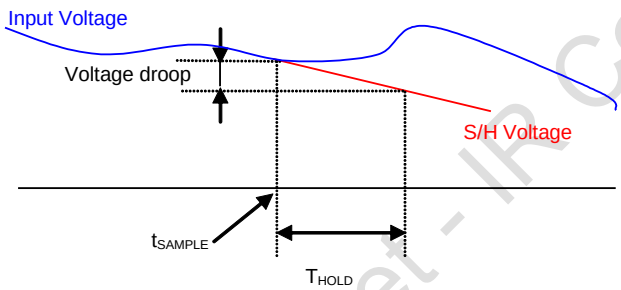

Figure 6 Voltage droop and S/H hold time

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6.3 Op amp AC Characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
OP_{SR}	OP amp slew rate	-	10 V/µsec	-	VDD1 = 3.3 V, CL = 33 pF (1)
OP_{IMP}	OP input impedance	-	10^8 Ω	-	(1) (2)
T_{SET}	Settling time	-	400 ns	-	VDD1 = 3.3 V, CL = 33 pF (1)

Table 11 Current Sensing OP Amp AC Characteristics

Note:

(1) Data guaranteed by design.

(2) To guarantee stability of the operational amplifier, it is recommended to load the output pin by a capacitor of 47pF, see Figure 7. Here only the single shunt current amplifier is shown but all op amp outputs should be loaded with this capacitor.

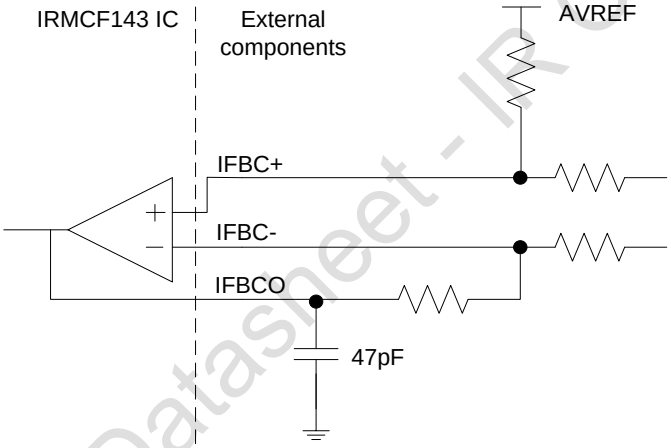

Figure 7 A capacitor of 47 pF is recommended at the output pin of all op amps.

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6.4 SYNC to SVPWM and A/D Conversion AC Timing

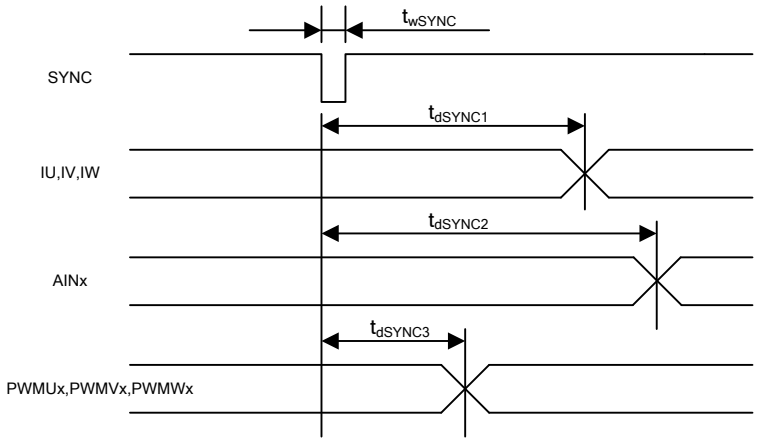

Figure 8 SYNC timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wSYNC}	SYNC pulse width	-	32	-	SYSCLK
t_{dSYNC1}	SYNC to current feedback conversion time	-	-	100	SYSCLK
t_{dSYNC2}	SYNC to AIN0-4 analog input conversion time	-	-	200	SYSCLK (1)
t_{dSYNC3}	SYNC to PWM output delay time	-	-	2	SYSCLK

Table 12. SYNC AC Characteristics

Note:
(1) AIN2 through AIN4 channels are converted once every 5 SYNC events

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6.5 GATEKILL to SVPWM AC Timing

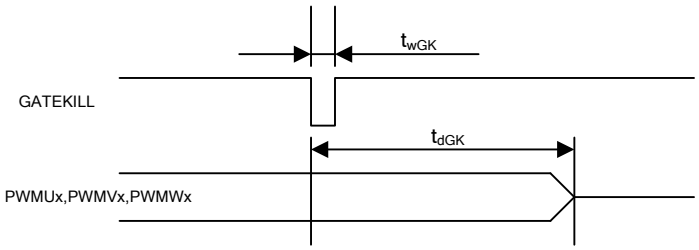

Figure 9 Gatekill timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wGK}	GATEKILL pulse width	32	-	-	SYSCLK
t_{dGK}	GATEKILL to PWM output delay	-	-	100	SYSCLK

Table 13. GATEKILL to SVPWM AC Timing

6.6 Itrip AC Timing

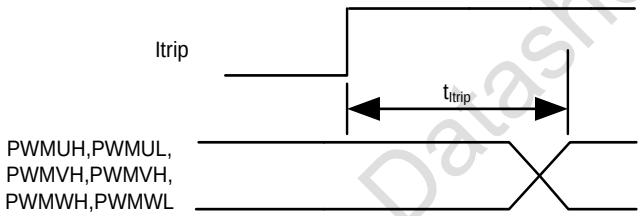

Figure 10 ITRIP timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{ITRIP}	Itrip propagation delay	-	-	100(sysclk)+1.0usec	SYSCLK+usec

Table 14. Itrip AC Timing

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6.7 Interrupt AC Timing

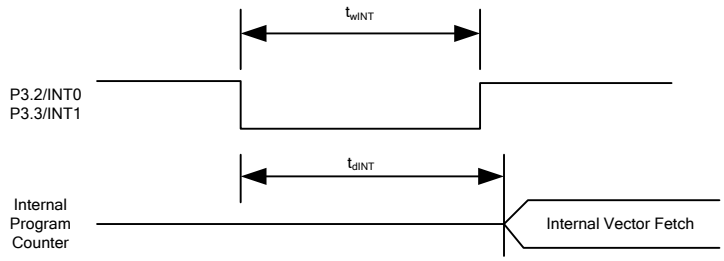

Figure 11 Interrupt timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wINT}	INT0, INT1 Interrupt Assertion Time	4	-	-	SYSCLK
t_{dINT}	INT0, INT1 latency	-	-	4	SYSCLK

Table 15. Interrupt AC Timing

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6.8 I²C AC Timing

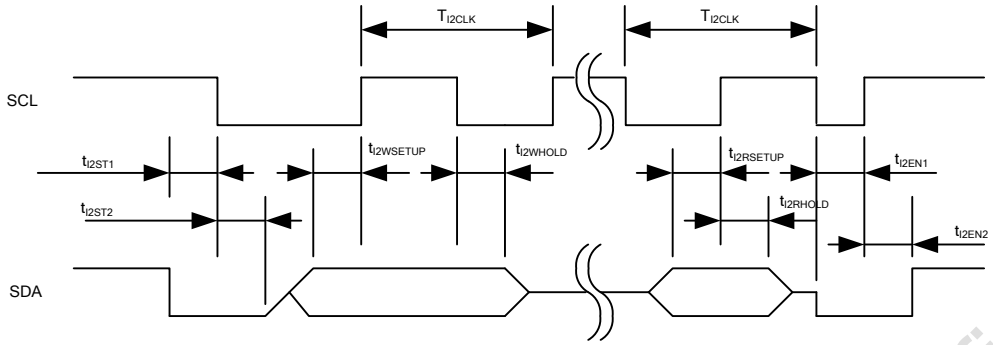

Figure 12 I²C Timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{I2CLK}	I²C clock period	10	-	8192	SYSCLK
t_{I2ST1}	I²C SDA start time	0.25	-	-	T_{I2CLK}
t_{I2ST2}	I²C SCL start time	0.25	-	-	T_{I2CLK}
$t_{I2WSETUP}$	I²C write setup time	0.25	-	-	T_{I2CLK}
$t_{I2WHOLD}$	I²C write hold time	0.25	-	-	T_{I2CLK}
$t_{I2RSETUP}$	I²C read setup time	I²C filter time(1)	-	-	SYSCLK
$t_{I2RHOLD}$	I²C read hold time	1	-	-	SYSCLK

Table 16. I²C AC Timing

Note:

(1) I²C read setup time is determined by the programmable filter time applied to I²C communication.

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6.9 SPI AC Timing

6.9.1 SPI Write AC timing

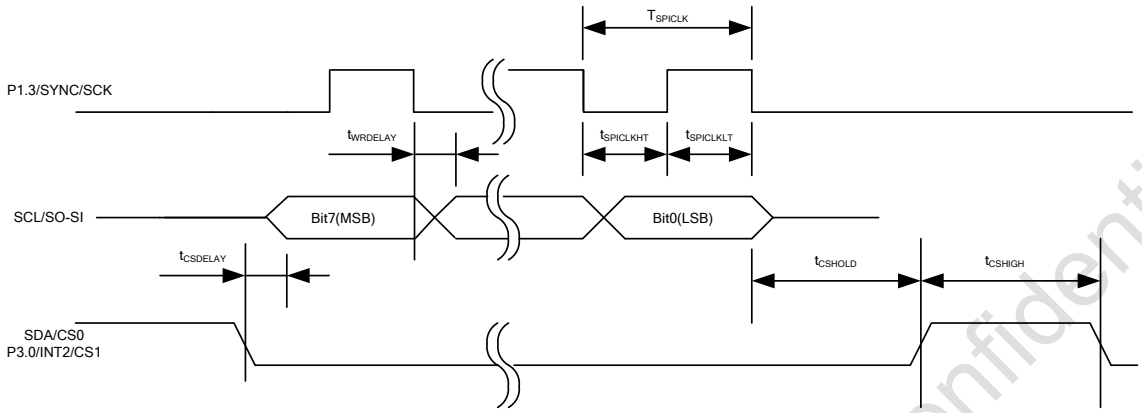

Figure 13 SPI write timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{SPICLK}	SPI clock period	4	-	-	SYSCLK
$t_{SPICLKHT}$	SPI clock high time	-	1/2	-	T_{SPICLK}
$t_{SPICLKLT}$	SPI clock low time	-	1/2	-	T_{SPICLK}
$t_{CSDELAY}$	CS to data delay time	-	-	10	nsec
$t_{WRDELAY}$	CLK falling edge to data delay time	-	-	10	nsec
t_{CSHIGH}	CS high time between two consecutive byte transfer	1	-	-	T_{SPICLK}
t_{CSHOLD}	CS hold time	-	1	-	T_{SPICLK}

Table 17. SPI Write AC Timing

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6.9.2 SPI Read AC Timing

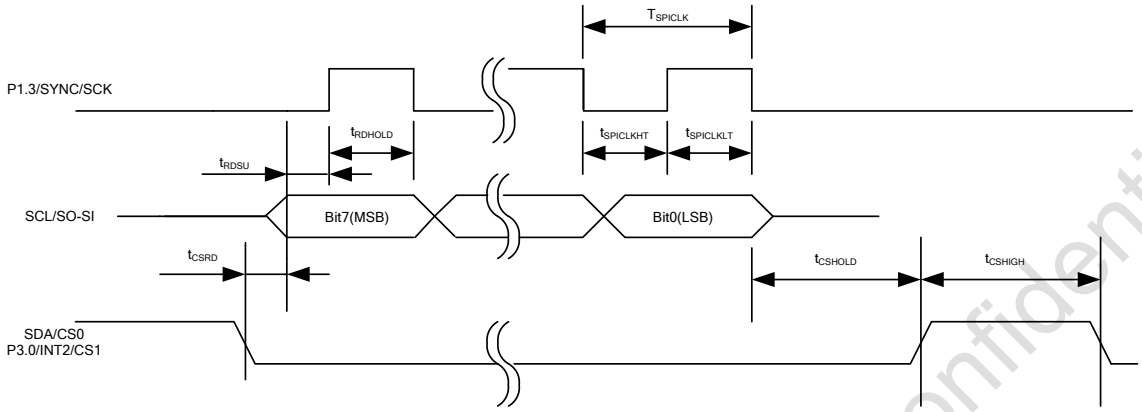

Figure 14 SPI read timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{SPICLK}	SPI clock period	4	-	-	SYSCLK
$t_{SPICLKHT}$	SPI clock high time	-	1/2	-	T_{SPICLK}
$t_{SPICLKLT}$	SPI clock low time	-	1/2	-	T_{SPICLK}
t_{CSRD}	CS to data delay time	-	-	10	nsec
t_{RDSU}	SPI read data setup time	10	-	-	nsec
t_{RDHOLD}	SPI read data hold time	10	-	-	nsec
t_{CSHIGH}	CS high time between two consecutive byte transfer	1	-	-	T_{SPICLK}
t_{CSHOLD}	CS hold time	-	1	-	T_{SPICLK}

Table 18. SPI Read AC Timing

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6.10 UART AC Timing

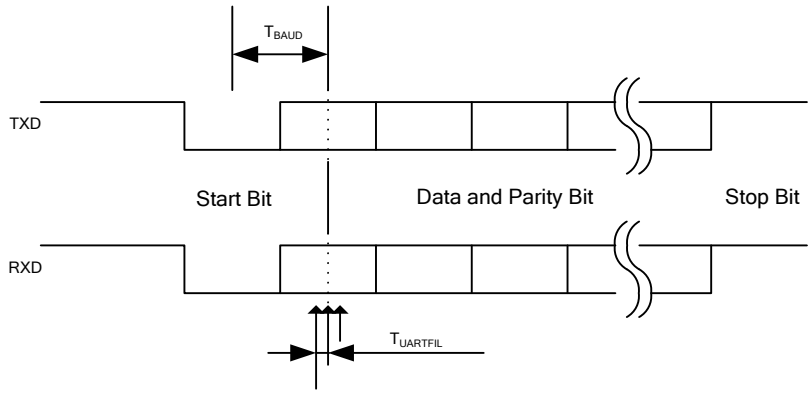

Figure 15 UART timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{BAUD}	Baud Rate Period	-	57600	-	bit/sec
$T_{UARTFIL}$	UART sampling filter period (1)	-	1/16	-	T_{BAUD}

Table 19. UART AC Timing

Note:

(1) Each bit including start and stop bit is sampled three times at center of a bit at an interval of 1/16 T_{BAUD}. If three sampled values do not agree, then UART noise error is generated.

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6.11 CAPTURE Input AC Timing

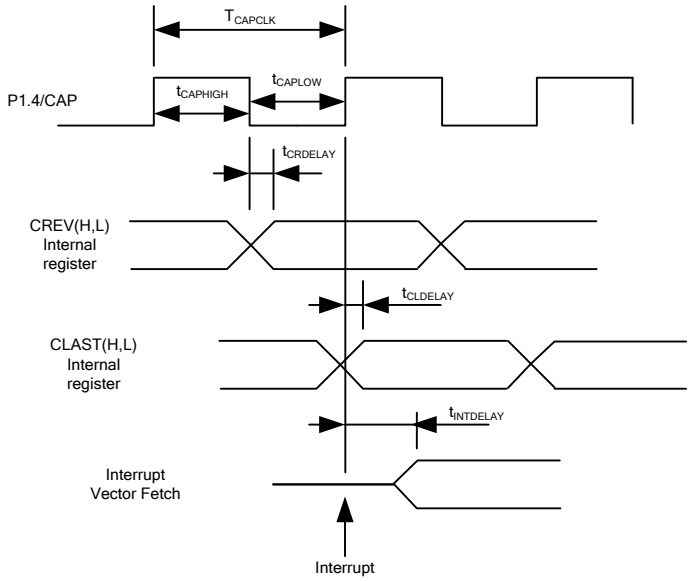

Figure 16 CAPTURE timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{CAPCLK}	CAPTURE input period	8	-	-	SYSCLK
$t_{CAPHIGH}$	CAPTURE input high time	4	-	-	SYSCLK
t_{CAPLOW}	CAPTURE input low time	4	-	-	SYSCLK
$t_{CRDELAY}$	CAPTURE falling edge to capture register latch time	-	-	4	SYSCLK
$t_{CLDELAY}$	CAPTURE rising edge to capture register latch time	-	-	4	SYSCLK
$t_{INTDELAY}$	CAPTURE input interrupt latency time	-	-	4	SYSCLK

Table 20. CAPTURE AC Timing

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6.12 JTAG AC Timing

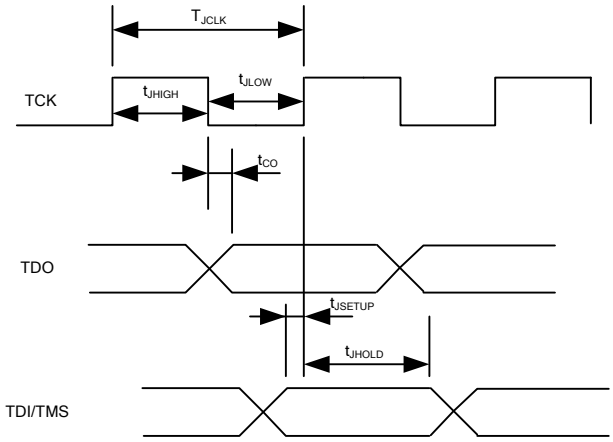

Figure 17 JTAG timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{JCLK}	TCK Period	-	-	50	MHz
t_{JHIGH}	TCK High Period	10	-	-	nsec
t_{JLOW}	TCK Low Period	10	-	-	nsec
t_{CO}	TCK to TDO propagation delay time	0	-	5	nsec
t_{JSETUP}	TDI/TMS setup time	4	-	-	nsec
t_{JHOLD}	TDI/TMS hold time	0	-	-	nsec

Table 21. JTAG AC Timing

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7 I/O Structure

The following figure shows the motor PWM output (PWMUH/PWMUL/PWMVH /PWMVL /PWMWH /PWMWL)

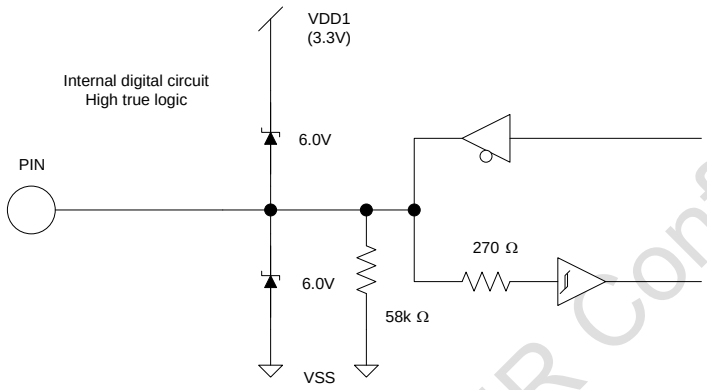

Figure 18 PWMUL/PWMUH/PWMVL/PWMVH/PWMWL/PWMWH output

The following figure shows the digital I/O structure except the motor PWM output

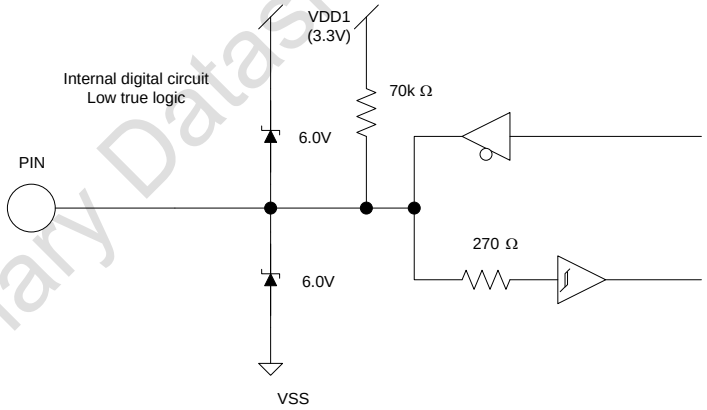

Figure 19 All digital I/O except motor PWM output

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The following figure shows RESET and GATEKILL I/O structure.

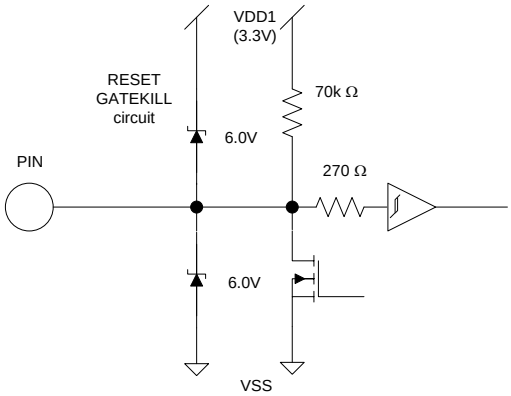

Figure 20 RESET, GATEKILL I/O

The following figure shows the analog input structure.

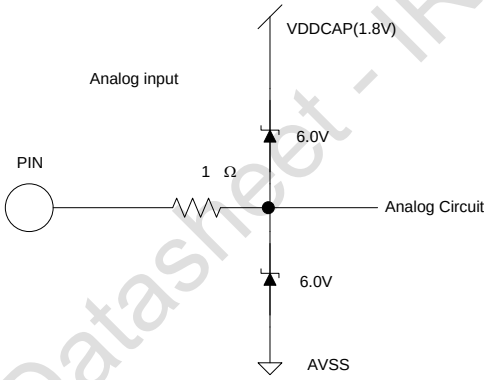

Figure 21 Analog input

The following figure shows all analog operational amplifier output pins and AREF pin I/O structure.

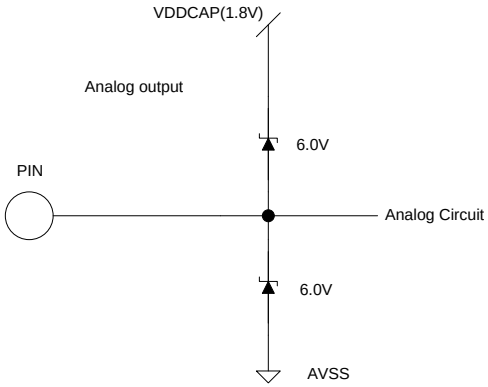

Figure 22 Analog operational amplifier output and AREF I/O structure

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The following figure shows the VSS,AVSS pin I/O structure

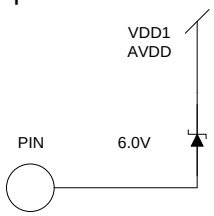

Figure 23 VSS,AVSS pin I/O structure

The following figure shows the VDD1,VDDCAP pin I/O structure

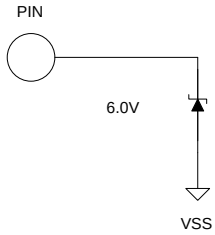

Figure 24 VDD1,VDDCAP pin I/O structure

The following figure shows the XTAL0 and XTAL1 pins structure

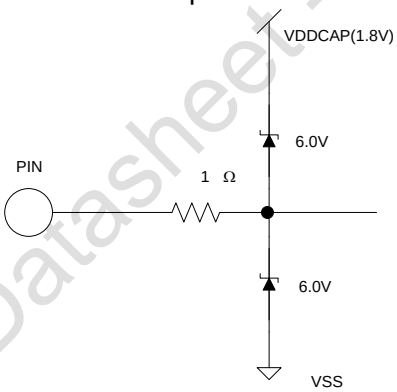

Figure 25 XTAL0/XTAL1 pins structure

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8 Pin List

Pin Number	Pin Name	Internal Pull-up /Pull-down	Pin Type	Description
1	XTAL0		I	Crystal input
2	XTAL1		O	Crystal output
3	P1.0/T2		I/O	Discrete programmable I/O or Timer/Counter 2 input
4	SCL/SO-SI		I/O	I^2C clock output (open drain, need pull up) or SPI data
5	SDA/CS0		I/O	I^2C data (open drain, need pull up) or SPI Chip Select 0
6	P1.3/SYNC/SCK		I/O	Discrete programmable I/O or SYNC output or SPI clock output
7	P1.4/CAP		I/O	Discrete programmable I/O or Capture timer input
8	P1.6		I/O	Discrete programmable I/O
9	P1.7			Discrete programmable I/O
10	VDD1		P	3.3V digital power
11	VSS		P	Digital common
12	VDDCAP		P	Internal 1.8V output, Capacitor(s) to be connected
13	P2.0/NMI		I/O	Discrete programmable I/O or Non-maskable Interrupt input
14	P3.2/INT0		I/O	Discrete programmable I/O or Interrupt 0 input
15	P2.2		I/O	Discrete programmable I/O
16	P2.3		I/O	Discrete programmable I/O
17	P2.5		I/O	Discrete programmable I/O
18	P2.6/AOPWM0		I/O	Discrete programmable I/O or PWM 0 digital output
19	P2.7/AOPWM1		I/O	Discrete programmable I/O or PWM 1 digital output
20	VACO		O	AC line voltage sensing OP amp output
21	VAC-		I	AC line voltage sensing OP amp input (-)
22	VAC+		I	AC line voltage sensing OP amp input (+)
23	AIN0		I	Analog input channel 0, 0-1.2V range, needs to be pulled down to AVSS if unused
24	AIN1		I	Analog input channel 1, 0-1.2V range, needs to be pulled down to AVSS if unused
25	AIN2		I	Analog input channel 2, 0-1.2V range, needs to be pulled down to AVSS if unused
26	AIN3		I	Analog input channel 3, 0-1.2V range, needs to be pulled down to AVSS if unused
27	AIN4		I	Analog input channel 4, 0-1.2V range, needs to be pulled down to AVSS if unused
28	IFB-		I	Single shunt current sensing OP amp input (-)
29	IFB+		I	Single shunt current sensing OP amp input (+)
30	IFBO		O	Single shunt current sensing OP amp output
31	CMEXT		O	Unbuffered 0.6V output. Capacitor needs to be connected.
32	AREF		O	Analog reference voltage output (0.6V)
33	IPFC-		I	PFC current sensing OP amp input -, 0-1.2V range, needs to be pulled down to AVSS if unused
34	IPFC+		I	PFC current sensing OP amp input +, 0-1.2V range, needs to be pulled down to AVSS if unused
35	IPFCO		O	PFC current sensing OP amp output, 0-1.2V range,
36	AVSS		P	Analog common

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Pin Number	Pin Name	Internal Pull-up /Pull-down	Pin Type	Description
37	VDDCAP		P	Internal 1.8V output, Capacitor(s) to be connected
38	VDD1		P	3.3V digital power
39	VSS		P	Digital common
40	P3.1/AOPWM2		I/O	Discrete programmable I/O or PWM 2 digital output
41	PWMWL	58 kΩ Pull down	O	PWM gate drive for phase W low side, configurable either high or low true.
42	PWMVL	58 kΩ Pull down	O	PWM gate drive for phase V low side, configurable either high or low true
43	PWMUL	58 kΩ Pull down	O	PWM gate drive for phase U low side, configurable either high or low true
44	PWMWH	58 kΩ Pull down	O	PWM gate drive for phase W high side, configurable either high or low true
45	P3.7		I/O	Discrete programmable I/O
46	P2.1		I/O	Discrete programmable I/O
47	P3.6		I/O	Discrete programmable I/O
48	PWMVH	58 kΩ Pull down	O	PWM gate drive for phase V high side, configurable either high or low true
49	PWMUH	58 kΩ Pull down	O	PWM gate drive for phase U high side, configurable either high or low true
50	P1.5		I/O	Discrete programmable I/O.
51	PFCPWM		I/O	PFC PWM gate drive , configurable either high or low
52	PFCGKILL	70 kΩ Pull up	I	PFCPWM shutdown input, active low input.
53	GATEKILL	70 kΩ Pull up	I	PWM shutdown input, 2-µsec digital filter, active low input.
54	P3.0/INT2/CS1	70 kΩ Pull up	I/O	Discrete programmable I/O or external interrupt 2 input or SPI Chip Select 1
55	P5.2/TMS		I/O	JTAG test mode input or input digital port
56	TDO		I/O	JTAG test data output
57	P5.1/TDI		I/O	JTAG test data input or input digital port
58	TCK		I	JTAG test clock
59	RESET		I/O	Reset, low true, Schmitt trigger input
60	P1.1/RXD		I/O	UART receiver input or Discrete programmable I/O
61	P1.1/RXD		I/O	UART transmitter output or Discrete programmable I/O
62	P3.4/T0		I/O	Discrete programmable I/O or Timer/Counter 2 input
63	P3.5/T1		I/O	Discrete programmable I/O or Timer/Counter 2 input
64	P3.3/INT1		I/O	Interrupt 1 input or Discrete I/O

Table 22. Pin List

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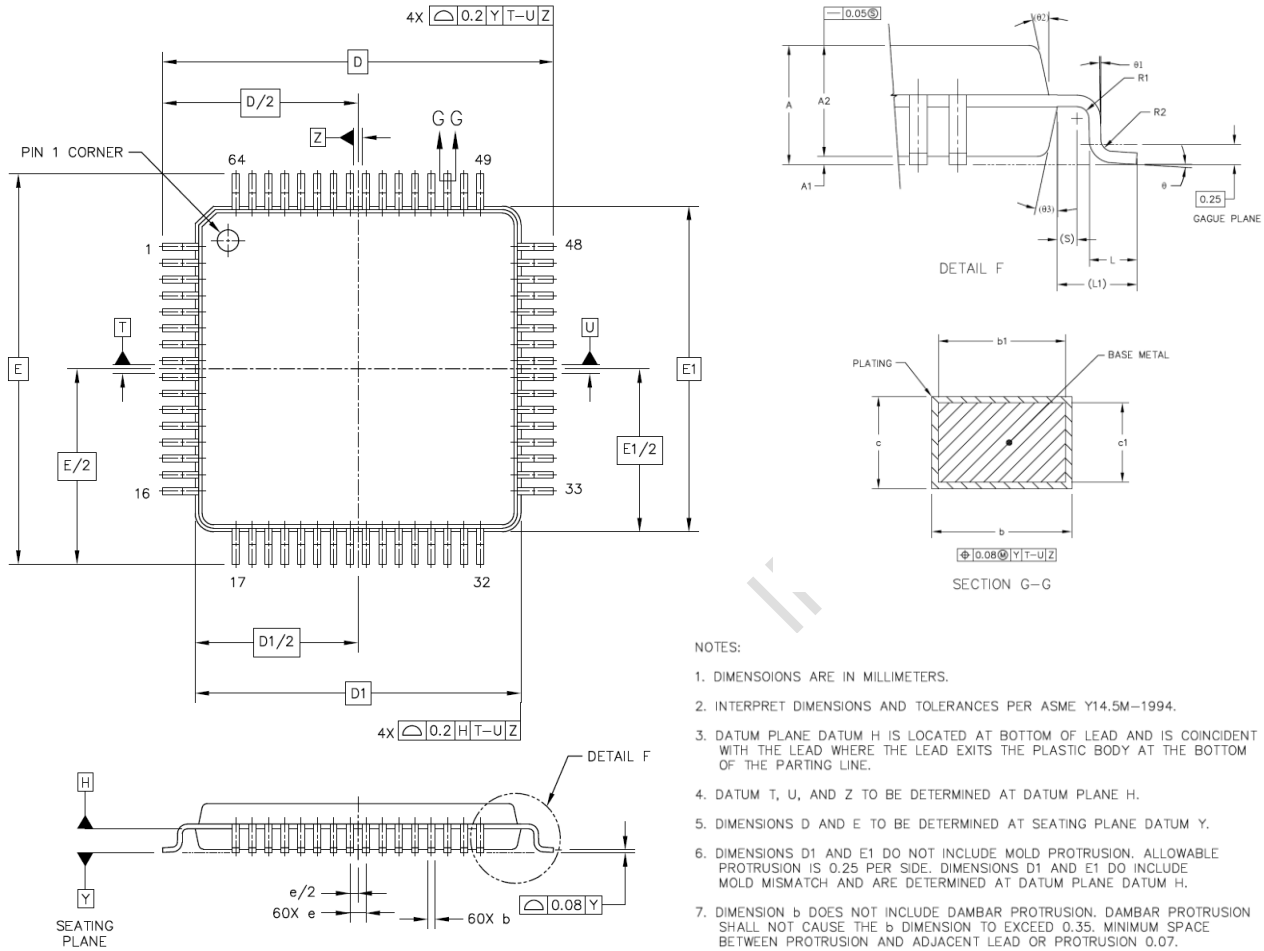
9 Package Dimensions



NOTES:

1. DIMENSOIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE DATUM H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

DIM	MIN	MAX	DIM	MIN	MAX	DIM	MIN	MAX
A	---	1.6	L1	1 REF				
A1	0.05	0.15	R1	0.1	0.2			
A2	1.35	1.45	R2	0.1	0.2			
b	0.17	0.27	S	0.2 REF				
b1	0.17	0.23	θ	0°	7°			
c	0.09	0.2	θ1	0°	---			
c1	0.09	0.16	θ2	12° REF				
D	12 BSC		θ3	12° REF				
D1	10 BSC							
e	0.5 BSC							
E	12 BSC							
E1	10 BSC							
L	0.45	0.75						

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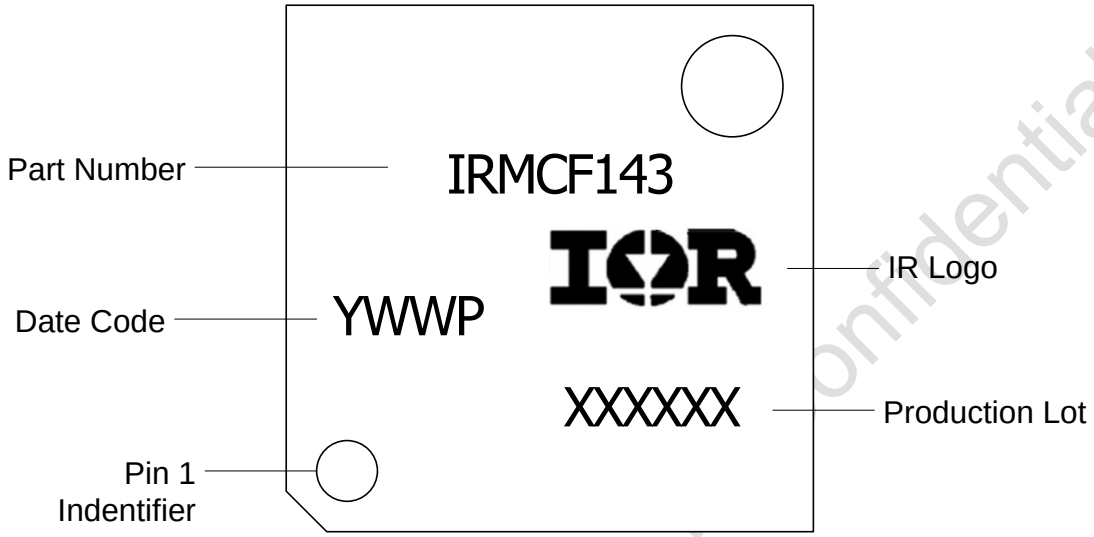
10 Part Marking Information



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