Atmel ATWINC1500-MR210PA

IEEE 802.11 b/g/n IoT Module

PRELIMINARY DATASHEET

Description

The ATWINC1500-MR210PA is a low-power consumption 802.11 b/g/n IoT (Internet of Things) module which is specifically optimized for low power IoT applications. The highly integrated module features small form factor (21.72mm x 14.73mm x3.5mm) while fully integrating Power Amplifier, LNA, Switch, Power Management and PCB antenna. With seamless roaming capabilities and advanced security, it could be interoperable with various vendors' 802.11b/g/n Access Points in wireless LAN. The module provides SPI and UART to interface to host controller.

Features

Key features of the ATWINC1500-MR210PA:

- IEEE 802.11 b/g/n RF/PH/MAC SoC
- IEEE 802.11 b/g/n (1x1) for up to 72Mbps
- Single spatial stream in 2.4Ghz RF band
- Integrated PA and T/R Switch
- Integrated PCB antenna
- Superior Sensitivity and Range via advanced PHY signal processing
- Advanced equalization and channel estimation
- Advanced carrier and timing synchronization

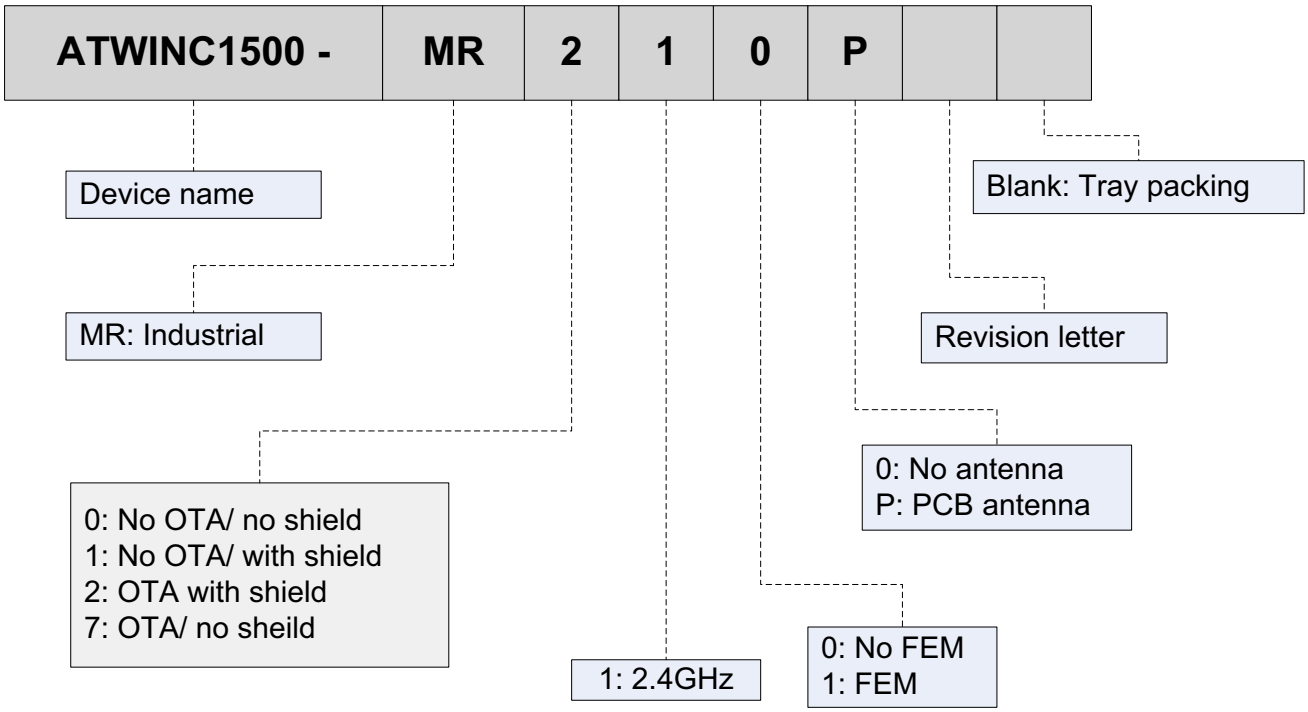
System features of the ATWINC1500-MR210PA:

- Wi-Fi Direct and Soft-AP support
- Supports IEEE 802.11 WEP, WPA, WPA2 Security
- On-chip memory management engine to reduce host load
- I/O operating voltage of 2.7V to 3.6V
- Operating temperature range of -30°C to +85°C
- Integrated Flash memory for system software
- SPI and UART host interfaces
- Power save modes:
  - 4µA Deep Power Down mode typical @3.3V I/O
  - 850µA Doze mode (Chip settings are preserved. Used for beacon monitoring mode)
  - On-chip low power sleep oscillator
  - Fast host wake-up from Doze mode by a pin or SPI transaction

- Fast boot options
  - On-Chip Boot ROM (Firmware instant boot)
  - SPI flash boot (firmware patches and state variables)
  - Low-leakage on-chip memory for state variables
  - Fast AP Re-Association (150ms)
- On-Chip Network Stack to off-load MCU
  - Integrated Network IP stack to minimize host CPU requirements
  - Network features TCP, UDP, DHCP, ARP, HTTP, SSL, and DNS
- Wi-Fi security WEP, WPA, WPA2 and WPS
- Small footprint host driver (4KB flash – less than 1KB RAM)

1. Ordering Information

Figure 1-1. ATWINC1500-MR210PA ordering information details

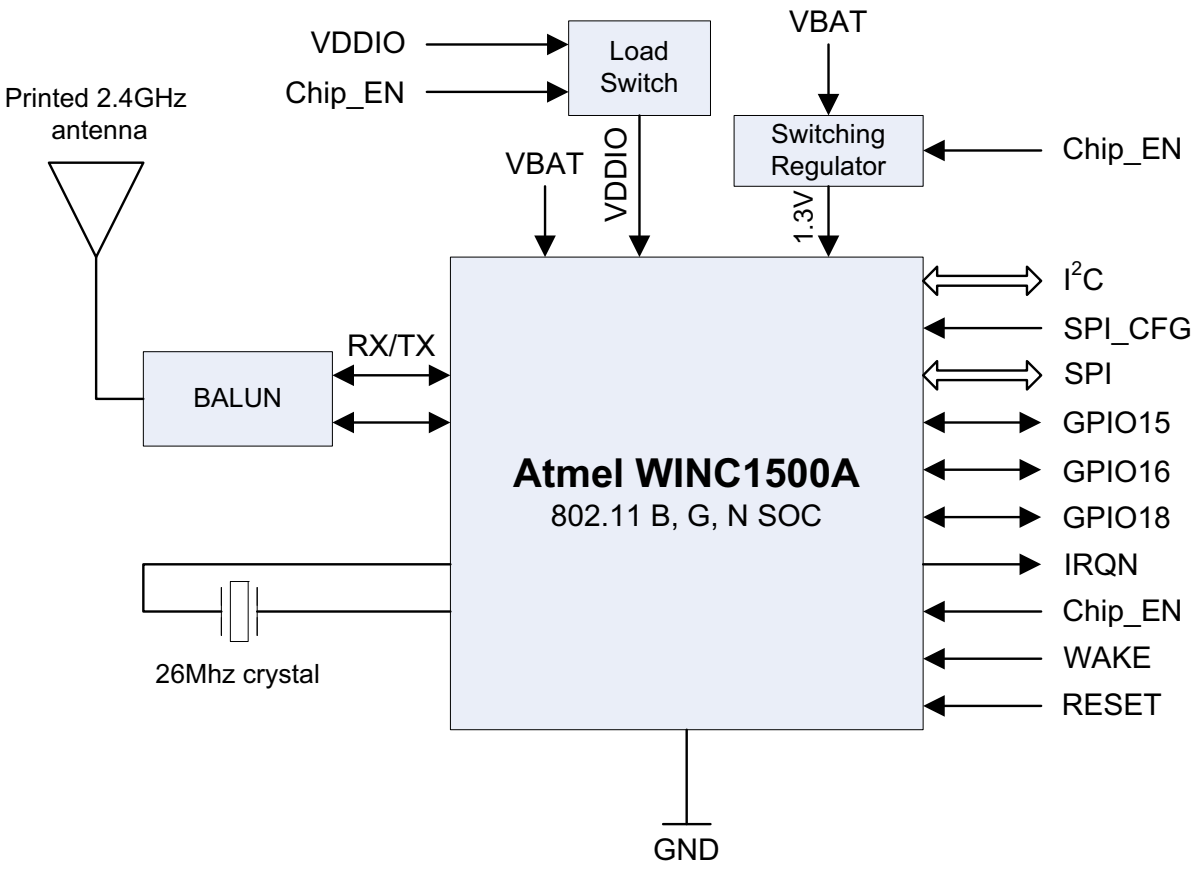


1.1 Regulatory certificates

The product is a pre-tested module certified to FCC Part 15, CE and TELEC.

2. Block Diagram

Figure 2-1. ATWINC1500-MR210P Block Diagram



3. General Specifications

3.1 Wi-Fi RF Specification

Table 3-1. Conditions: VBAT=3.6V; VDDIO=3.3V; Temp: 25°C

Feature	Description
Module part number	ATWINC1500-MR210P
WLAN standard	IEEE 802.11b/g/n, Wi-Fi compliant
Host interface	SPI, UART
Dimension	L x W x H: 21.72 x 14.73 x 3.5 (typical) mm
Frequency range	2.412GHz ~ 2.4835GHz (2.4GHz ISM Band)
Number of channels	11 for North America, 13 for Europe, and 14 for Japan
Modulation	802.11b: DQPSK, DBPSK, CCK
	802.11g/n: OFDM /64-QAM,16-QAM, QPSK, BPSK

Table 3-1. Conditions: VBAT=3.6V; VDDIO=3.3V; Temp: 25°C (Continued)

Feature	Description
Output power	802.11b /11Mbps: 19dBm ± 1dB
	802.11g /54Mbps: 15.5dBm ± 1dB @ EVM -28dB
	802.11n /65Mbps: 13dBm ± 1dB @ EVM -30dB
Receive Sensitivity (11n, 20MHz) @10% PER	▶ MCS=0 PER @ -90dBm ± 1dB
	▶ MCS=1 PER @ -86dBm ± 1dB
	▶ MCS=2 PER @ -84dBm ± 1dB
	▶ MCS=3 PER @ -81.5dBm ± 1dB
	▶ MCS=4 PER @ -78dBm ± 1dB
	▶ MCS=5 PER @ -74dBm± 1dB
	▶ MCS=6 PER @ -72.5dBm ± 1dB
	▶ MCS=7 PER @ -71.5dBm ± 1dB
Receive Sensitivity (11g) @10% PER	▶ 6Mbps PER @ -91dBm± 1dB
	▶ 9Mbps PER @ -89dBm ± 1dB
	▶ 12Mbps PER @ -88.5dBm ± 1dB
	▶ 18Mbps PER @ -86.5dBm ± 1dB
	▶ 24Mbps PER @ -84dBm ± 1dB
	▶ 36Mbps PER @ -78.5dBm ± 1dB
	▶ 48Mbps PER @ -77dBm ± 1dB
	▶ 54Mbps PER @ -75dBm ± 1dB
Receive Sensitivity (11b) @8% PER	▶ 1Mbps PER @ -98dBm ± 1dB
	▶ 2Mbps PER @ -95dBm ± 1dB
	▶ 5.5Mbps PER @ -93dBm ± 1dB
	▶ 11Mbps PER @ -89dBm ± 1dB
Data rate	802.11b: 1, 2, 5.5, 11Mbps
	802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
Data rate (20MHz, normal GI, 800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data rate (20MHz, short GI, 400ns)	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, 72.2Mbps
Maximum input level	802.11b: 0dBm typical
	802.11g/n: -5dBm typical
Operating temperature	-30°C to 85°C

Table 3-1. Conditions: VBAT=3.6V; VDDIO=3.3V; Temp: 25°C (Continued)

Feature	Description
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing
	Storage Humidity 5% to 95% Non-Condensing

3.2 Voltages

3.2.1 Absolute Maximum Ratings

Table 3-2. Voltages

Symbol	Description	Min	Typical	Max	Unit
VBAT	Input supply voltage	-0.3		5.0	V
VDDIO	I/O voltage	-0.3		4.6	V

3.2.2 Recommended Operating Ratings

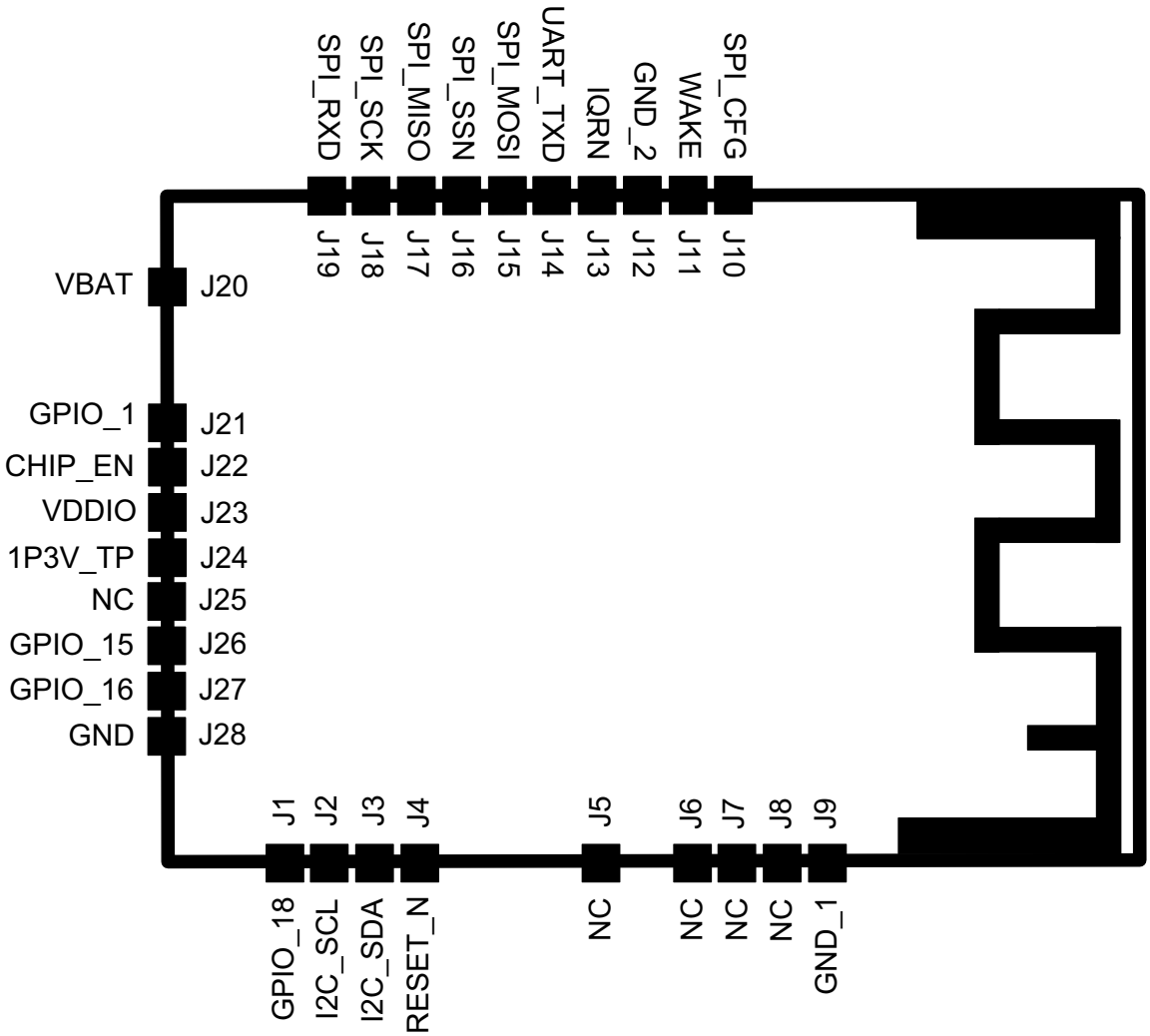
Table 3-3. Recommended Operating Ratings

Symbol	Test conditions	Min	Typical	Max	Unit
VBAT	-30°C - +85°C	3.0	3.6	4.2	V
VDDIO	-30°C - +85°C	2.7	3.3	3.6	V

4. Pin Assignments

4.1 Top View

Figure 4-1. Top View



4.2 Pin Descriptions

Table 4-1. Pin Descriptions

Pin #	Pin Name	Type	Description	Programmable Pull-up Resistor
1	GPIO_18	I/O	General purpose I/O.	YES
2	I2C_SCL	I/O	I^2C Slave Clock. Currently used only for Atmel debug. Not for customer use. Leave unconnected.	YES
3	I2C_SDA	I/O	I^2C Slave Data. Currently used only for Atmel debug. Not for customer use. Leave unconnected.	YES

Table 4-1. Pin Descriptions (Continued)

Pin #	Pin Name	Type	Description	Programmable Pull-up Resistor
4	RESET_N	I	Active-Low Hard Reset. When asserted to a low level, the module will be placed in a reset state. When asserted to a high level, the module will run normally. Connect to a host output that defaults low at power up. If the host output is tri-stated, add a 1MΩ pull-down resistor to ensure a low level at power up.	NO
5	NC	-	No connect	
6	NC	-	No connect	
7	NC	-	No connect	
8	NC	-	No connect	
9	GND_1	-	GND	
10	SPI_CFG	I	Tie to VDDIO through a 1MΩ resistor to enable the SPI interface	NO
11	WAKE	I	Host Wake control. Can be used to wake up the module from Doze mode. Connect to a host GPIO.	NO
12	GND_2	-	GND	
13	IRQN	O	ATWINC1500-MR210PA Device Interrupt output. Connect to host interrupt input pin.	NO
14	UART_TXD	O	UART Transmit Output from ATWINC1500-MR210P	YES
15	SPI_RXD	I	SPI MOSI (Master Out Slave In) pin	YES
16	SPI_SSN	I	SPI Slave Select. Active low	YES
17	SPI_TXD	O	SPI MISO (Master In Slave Out) pin	YES
18	SPI_CLK	I	SPI Clock	YES
19	UART_RXD	I	UART Receive input to ATWINC1500-MR210P	YES
20	VBATT	-	Battery power supply	
21	GPIO_1	I	General Purpose I/O	YES
22	CHIP_EN	I	Module enable. High level enables module, low level places module in Power Down mode. Connect to a host Output that defaults low at power up. If the host output is tri-stated, add a 1M ohm pull-down resistor to ensure a low level at power up.	NO
23	VDDIO	-	I/O Power Supply. Must match host I/O voltage	
24	1P3V_TP	-	1.3V VDD Core Test Point. Leave unconnected	
25	NC	-	No connect	
26	GPIO_15	I/O	General purpose I/O	YES
27	GPIO_16	I/O	General purpose I/O	YES
28	GND_3	-	GND	

5. Host Interfaces

5.1 I²C Interface

5.1.1 Overview

Atmel ATWINC1500-MR210P provides an I²C bus slave that allows the host processor to read or write any register in the chip. The ATWINC1500-MR210P supports I²C bus Version 2.1 - 2000.

The I²C interface, used primarily for control, is a two-wire serial interface consisting of a serial data line (SDA, Pin 17) and a serial clock (SCL, Pin 18). It responds to the seven bit address value 0x60. The ATWINC1500-MR210P I²C interface can operate in standard mode (with data rates up to 100Kb/s) and fast mode (with data rates up to 400Kb/s).

The I²C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400pF. Data is transmitted in byte packages.

For specific information, please refer to the Philips Specification entitled "The I²C -Bus Specification, Version 2.1".

5.1.2 I²C Timing

The I²C is provided in Figure 5-1 and in Table 5-1 on page 9.

Figure 5-1. ATWINC1500-MR210P I²C Timing Diagram

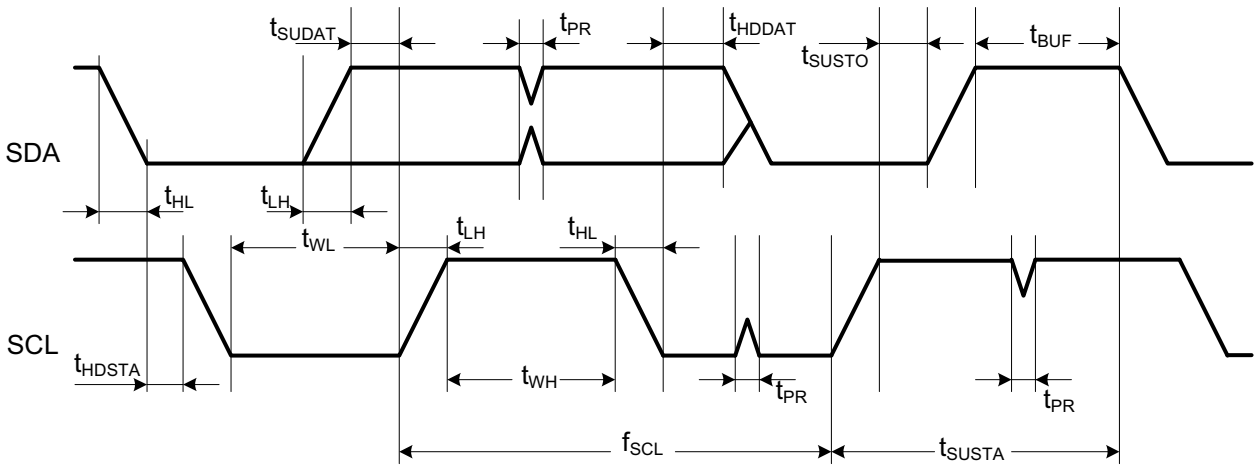


Table 5-1. ATWINC1500-MR210P I²C Timing Parameters

Parameter	Symbol	Min	Max	Units	Remarks
SCL clock frequency	f_{SCL}	0	400	kHz	
SCL low pulse width	t_{WL}	1.3		µs	
SCL high pulse width	t_{WH}	0.6		µs	

Table 5-1. ATWINC1500-MR210P I²C Timing Parameters (Continued)

Parameter	Symbol	Min	Max	Units	Remarks
SCL, SDA fall time	t_{HL}		300	ns	
SCL, SDA rise time	t_{LH}		300	ns	This is dictated by external components
START setup time	t_{SUSTA}	0.6		µs	
START hold time	t_{HDSTA}	0.6		µs	
SDA setup Time	t_{SUDAT}	100		ns	
SDA hold time	t_{HDDAT}	0		ns	Slave and Master default
		40		ns	Master programming option
STOP setup time	t_{SUSTO}	0.6		µs	
Bus free time between STOP and START	t_{BUF}	1.3		µs	
Glitch pulse reject	t_{PR}	0	50	ns	

5.2 SPI Interface

5.2.1 Overview

Atmel ATWINC1500-MR210P has a Serial Peripheral Interface (SPI) that operates as a SPI slave. The SPI interface can be used for control and for serial I/O of 802.11 data. The SPI pins are mapped as shown in Table 5-2. The SPI is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 10 (SPI_CFG) is tied to VDDIO.

Table 5-2. ATWINC1500-MR210P SPI Interface Pin Mapping

Pin #	SPI Function
10	CFG: Must be tied to VDDIO
16	SSN: Active low slave select
15	MOSI(RXD): Serial Data Receive
18	SCK: Serial Clock
17	MISO(TXD): Serial Data Transmit

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

The SPI SSN, MOSI, MISO and SCK pins of the ATWINC1500-MR210P have internal programmable pull-up resistors (See “Programmable Pull Up Resistors” on page 14). These resistors should be programmed to be disabled. Otherwise, if any of the SPI pins are driven to a low level while the ATWINC1500-MR210P is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module.

5.2.2 SPI Timing

The SPI timing is provided in Figure 5-2 and in Table 5-3 on page 11

Figure 5-2. SPI Timing Diagram (SPI Mode CPOL=0, CPHA=0)

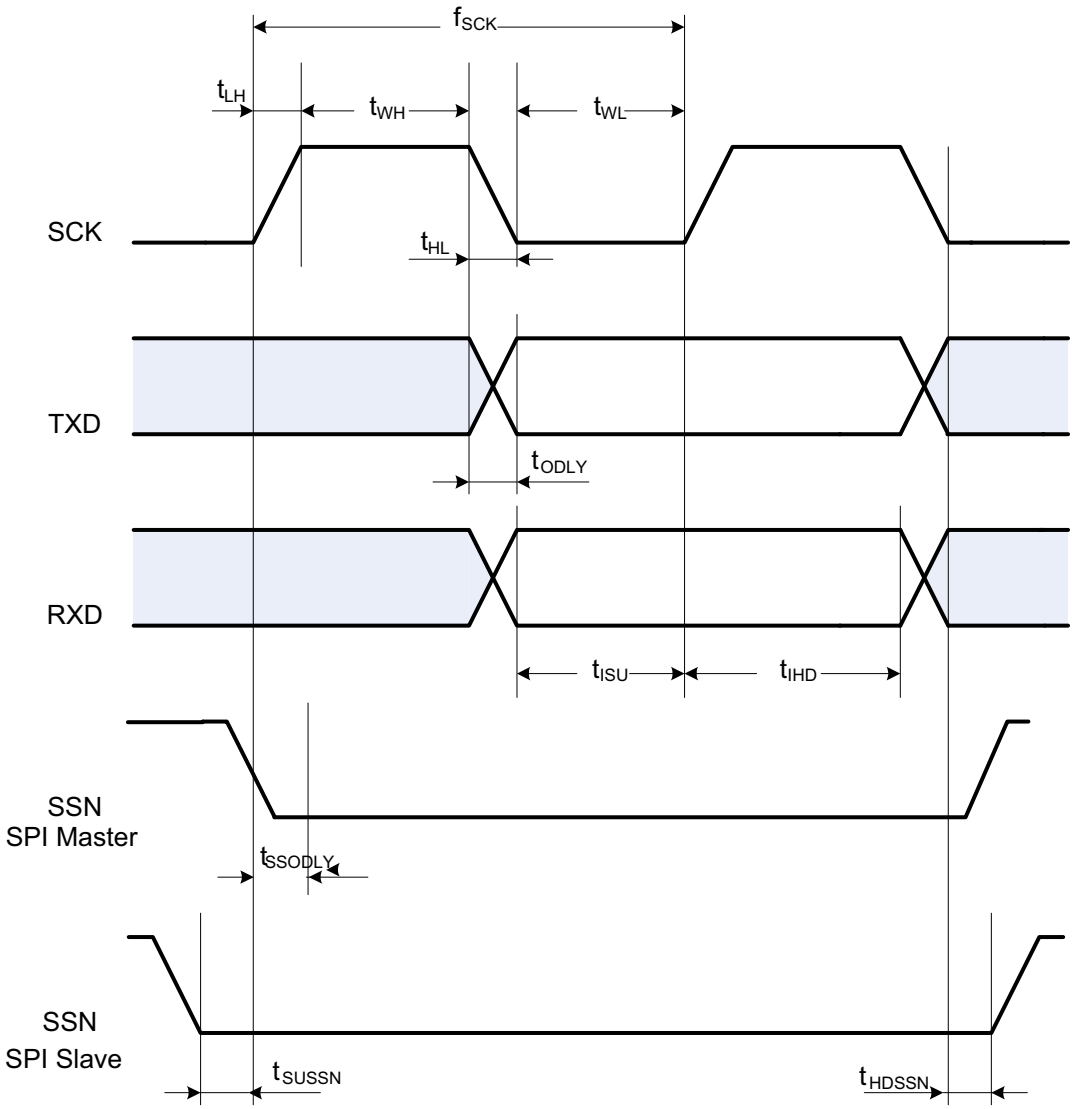


Table 5-3. SPI Slave Timing Parameters

Parameter	Symbol	Min	Max	Units
Clock input frequency	f_{SCK}		48	MHz
Clock low pulse width	t_{WL}	15		ns
Clock high pulse width	t_{WH}	15		ns
Clock rise time	t_{LH}		10	ns
Clock fall time	t_{HL}		10	ns
Input setup time	t_{ISU}	5		ns

Table 5-3. SPI Slave Timing Parameters (Continued)

Parameter	Symbol	Min	Max	Units
Input hold time	t_{IHD}	5		ns
Output delay	t_{ODLY}	0	20	ns
Slave select setup time	t_{SUSSN}	5		ns
Slave select hold time	t_{HDSSN}	5		ns

5.3 UART Interface

Atmel ATWINC1500-MR210P has a Universal Asynchronous Receiver / Transmitter (UART) interface available on pins J14 and J19. It can be used for control or data transfer if the baud rate is sufficient for a given application. The UART is compatible with the RS-232 standard, where ATWINC1500-MR210PA operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

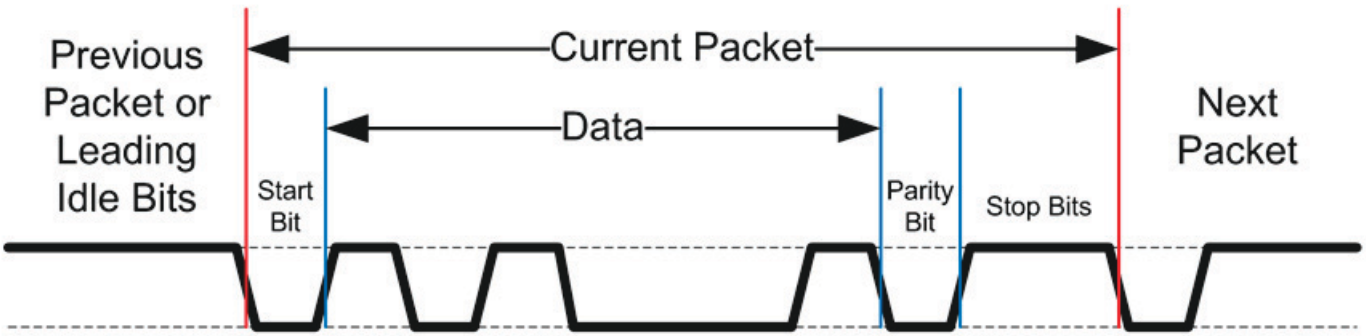
The UART features programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The UART input clock is selectable between 10MHz, 5MHz, 2.5MHz, and 1.25MHz. The clock divider value is programmable as 13 integer bits and 3 fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of 10MHz / 8.0 = 1.25MBd.

The UART can be configured for seven or eight bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also has Rx and Tx FIFOs, which ensure reliable high speed reception and low software overhead transmission. FIFO size is 4 x 8 for both Rx and Tx direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in Figure 5-3 on page 12. This example shows 7-bit data (0x45), odd parity, and two stop bits.

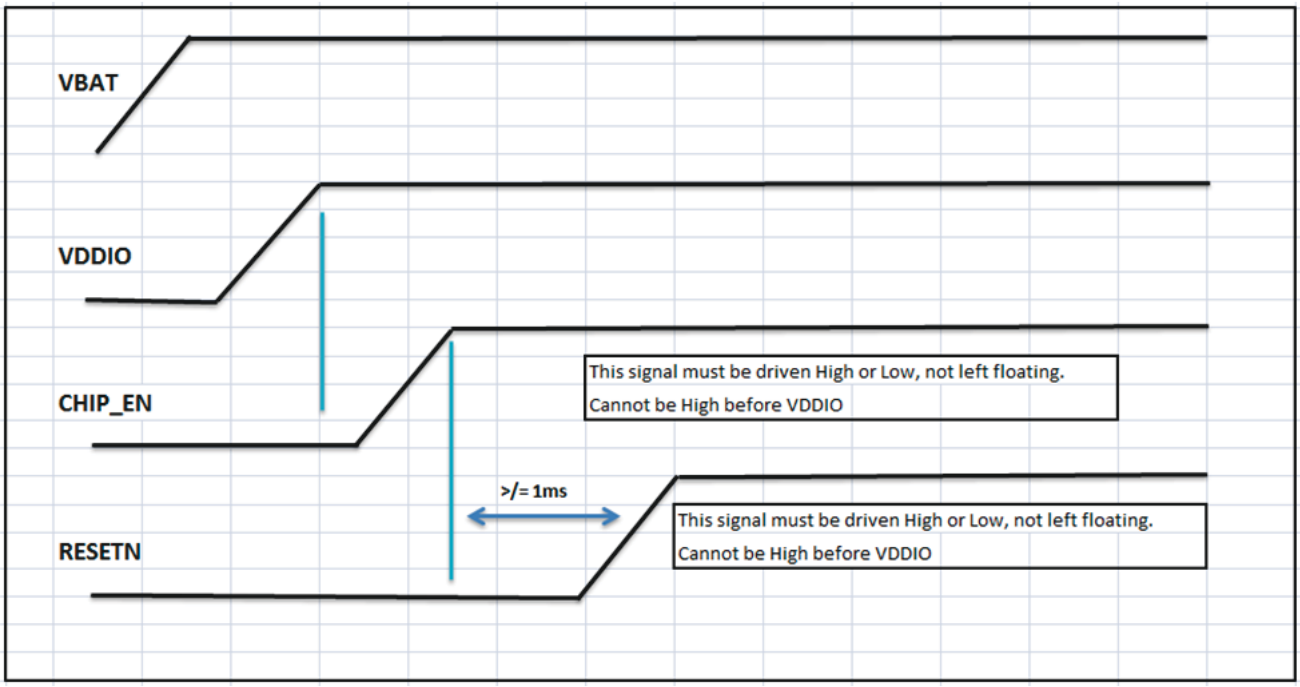
See the ATWINC1500-MR210PA Programming Guide for information on configuring the UART.

Figure 5-3. Example of UART Rx or Tx packet



5.4 Host Interface Power-up Sequence Timing Diagram

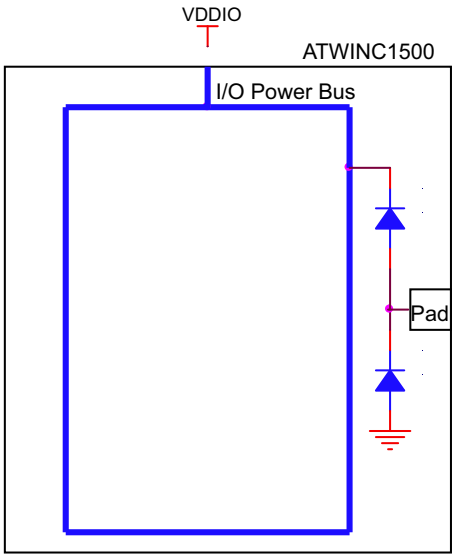
Figure 5-4. Host Interface Power up Sequence Timing Diagram



6. VDDIO Load Switch

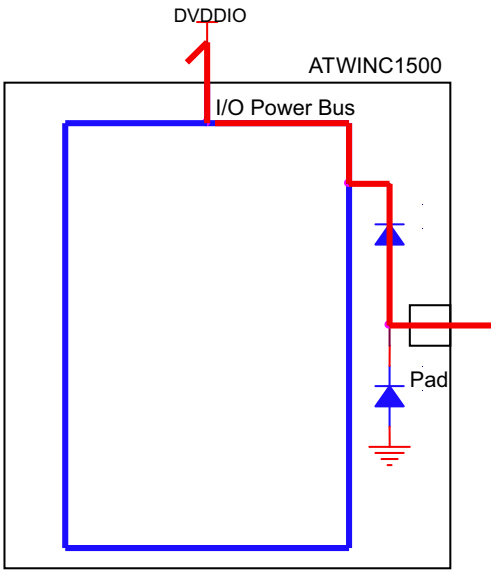
The ATWINC1500-MR210P module is designed with a load switch in series with the VDDIO supply. The load switch is controlled by the Chip_En pin of the module (Module pin 22). When Chip_En is high, the load switch is turned on. When Chip_En is low the load switch is open and VDDIO is disconnected from the ATWINC1500-MR210P. When the VDDIO supply to the ATWINC1500-MR210PA is disconnected it is important that none of the pins to the ATWINC1500-MR210PA is in a high state. Figure 6-1 on page 14 shows the ESD structure of the pins of the ATWINC1500 and Figure 6-2 on page 14 shows the current path through the ESD diode from a pin that is being driven high to the VDDIO supply of the device. In effect, if VDDIO is disconnected from the external power supply and a high level is driven on to a pad of the device, the device will be powered up through the pad.

Figure 6-1. ATWINC1500 Pad ESD structure



This shows why it is important that any time Chip_En to the module is low, all pins interfacing to the module must not be driven or pulled high. They should either be set to a low level or high impedance state. This means that if any external pull-up resistors are attached to any pins they should be disconnected from the supply when Chip_En is low.

Figure 6-2. Current Path through ESD diode



7. Notes On Interfacing To The ATWINC1500-MR210P

7.1 Programmable Pull Up Resistors

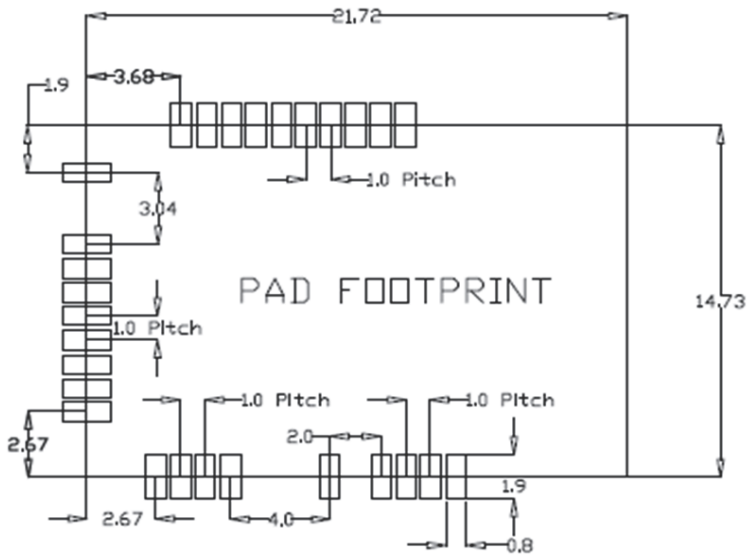
The ATWINC1500-MR210PA provides programmable pull-up resistors on various pins. The purpose of these resistors is to keep any unused input pins from floating which can cause excess current to flow through the input buffer from the VDDIO supply. Any unused module pin on the ATWINC1500-MR210P should leave these pull-up resistors enabled so the pin will not float. The default state at power up is for the pull-up resistor to be

enabled. However, any pin which is used should have the pull-up resistor disabled. The reason for this is that if any pins are driven to a low level while the ATWINC1500-MR210P is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module. Since the value of the pull-up resistor is approximately 100KΩ, the current through any pull-up resistor that is being driven low will be VDDIO/100K. For VDDIO = 3.3V, the current through each pull-up resistor that is driven low would be approximately 3.3V/100K = 33µA. Pins which are used and have had the programmable pull-up resistor disabled should always be actively driven to either a high or low level and not be allowed to float.

See the ATWINC1500-MR210PA Programming Guide for information on enabling/disabling the programmable pull up resistors.

8. Recommended Footprint (Unit: mm)

Figure 8-1. Footprint Drawing



9. RF Performance Placement Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

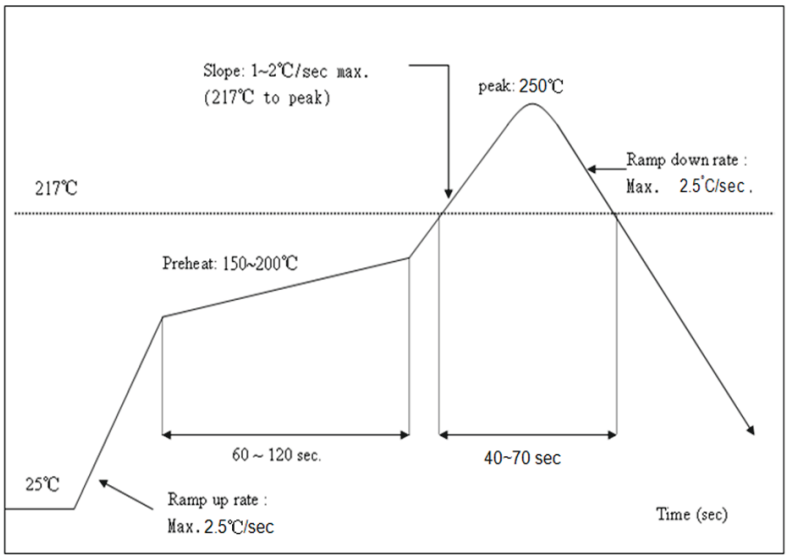
- Module must be placed on main board - printed antenna area must overlap with the carrier board. The portion of the module containing the antenna should not stick out over the edge of the main board. The antenna is designed to work properly when it is sitting directly on top of a 1.5mm thick printed circuit board.
- If the module is placed at the edge of the main board, a minimum 22mm by 5mm area directly under the an-tenna must be clear of all metal on all layers of the board. "In-land" placement is acceptable; however deep-ness of keep-out area must grove to: module edge to main board edge plus 5mm. DO NOT PLACE MODULE IN THE MIDDLE OF THE MAIN BOARD OR FAR AWAY FROM THE MAIN BOARD EDGE.
- Keep away from antenna, as far as possible, large metal objects to avoid electromagnetic field blocking.
- Do not enclose the antenna within a metal shield.
- Keep any components which may radiate noise or signals within the 2.4GHz - 2.5GHz frequency band far away from the antenna or better yet, shield those components. Any noise radiated from the main board in this frequency band will degrade the sensitivity of the module.
- Please contact Atmel for assistance if any other placement is required.

10. Recommended Reflow Profile

Referred to IPC/JEDEC standard. Peak Temperature: <250°C

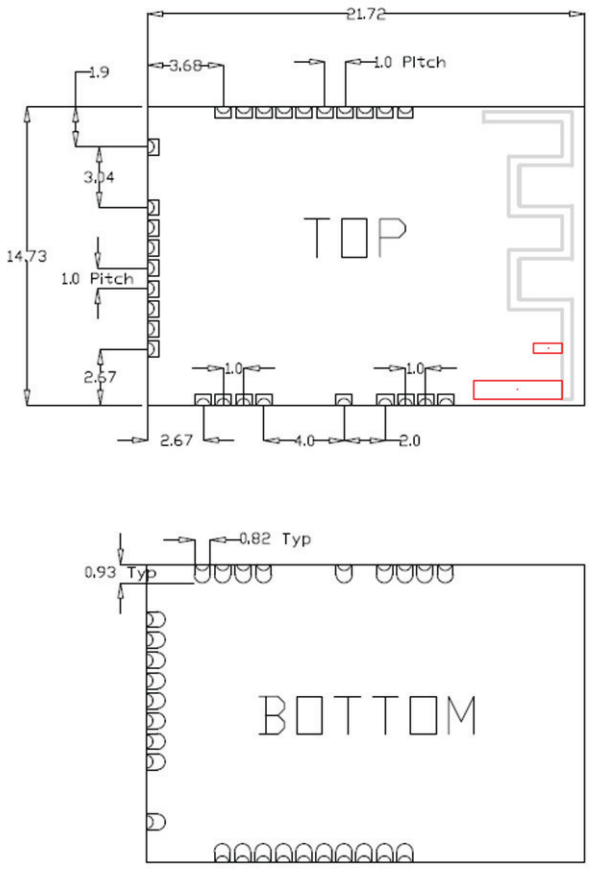
Number of times: 2 times maximum

Figure 10-1. Typical re-flow profile



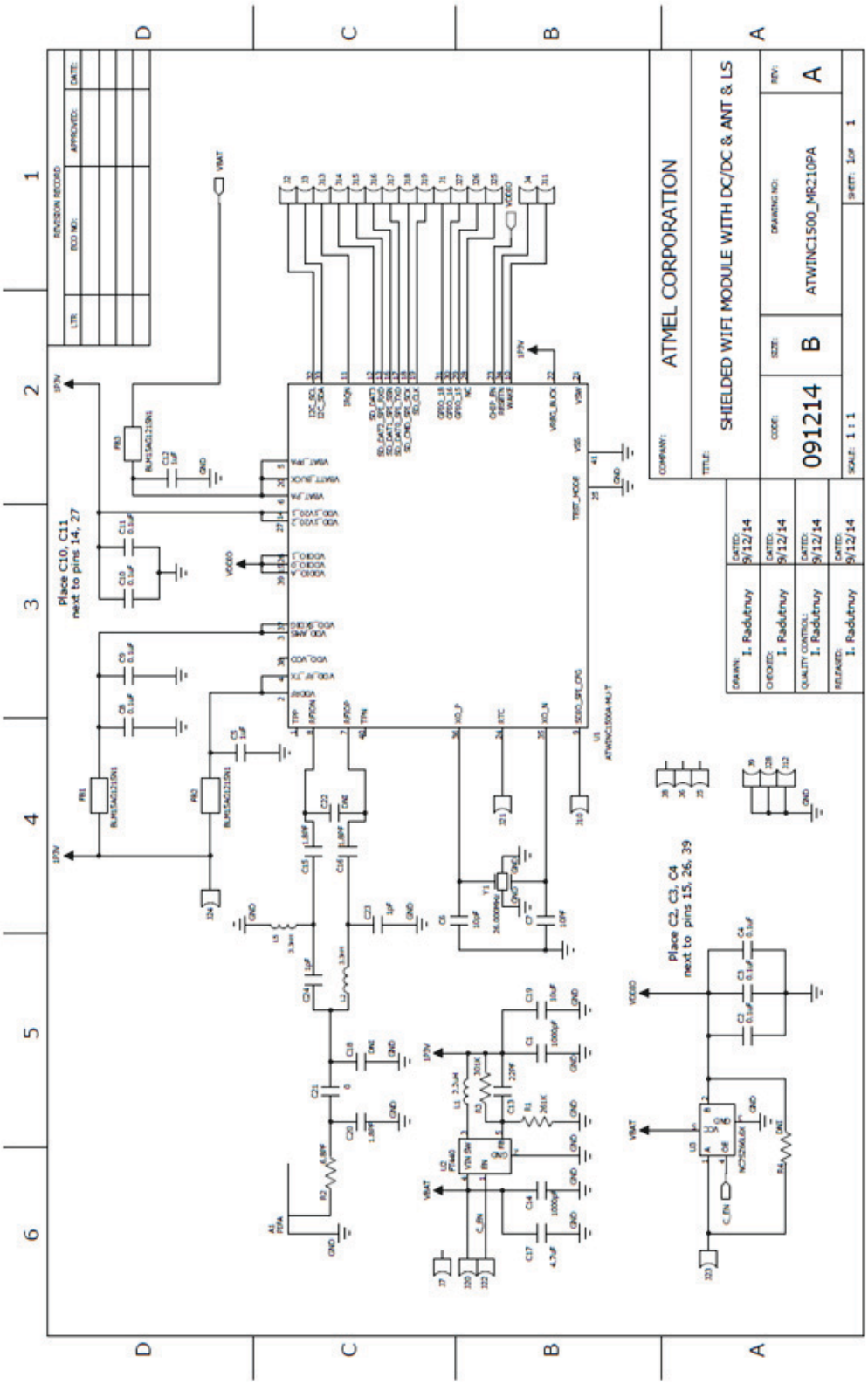
11. Module Outline Drawings

Figure 11-1. Module Drawings - Top and Bottom Views (unit = mm)



12. Module Schematic

Figure 12-1. ATWINC1500-MR210PA Schematic



13. Module Bill of Materials (BOM)

Table 13-1. ATWINC1500-MR210PA Bill of Material

WiFi shielded module with DC/DC, discrete balun, load switch and printed antenna Revised: Friday, September 11, 2014

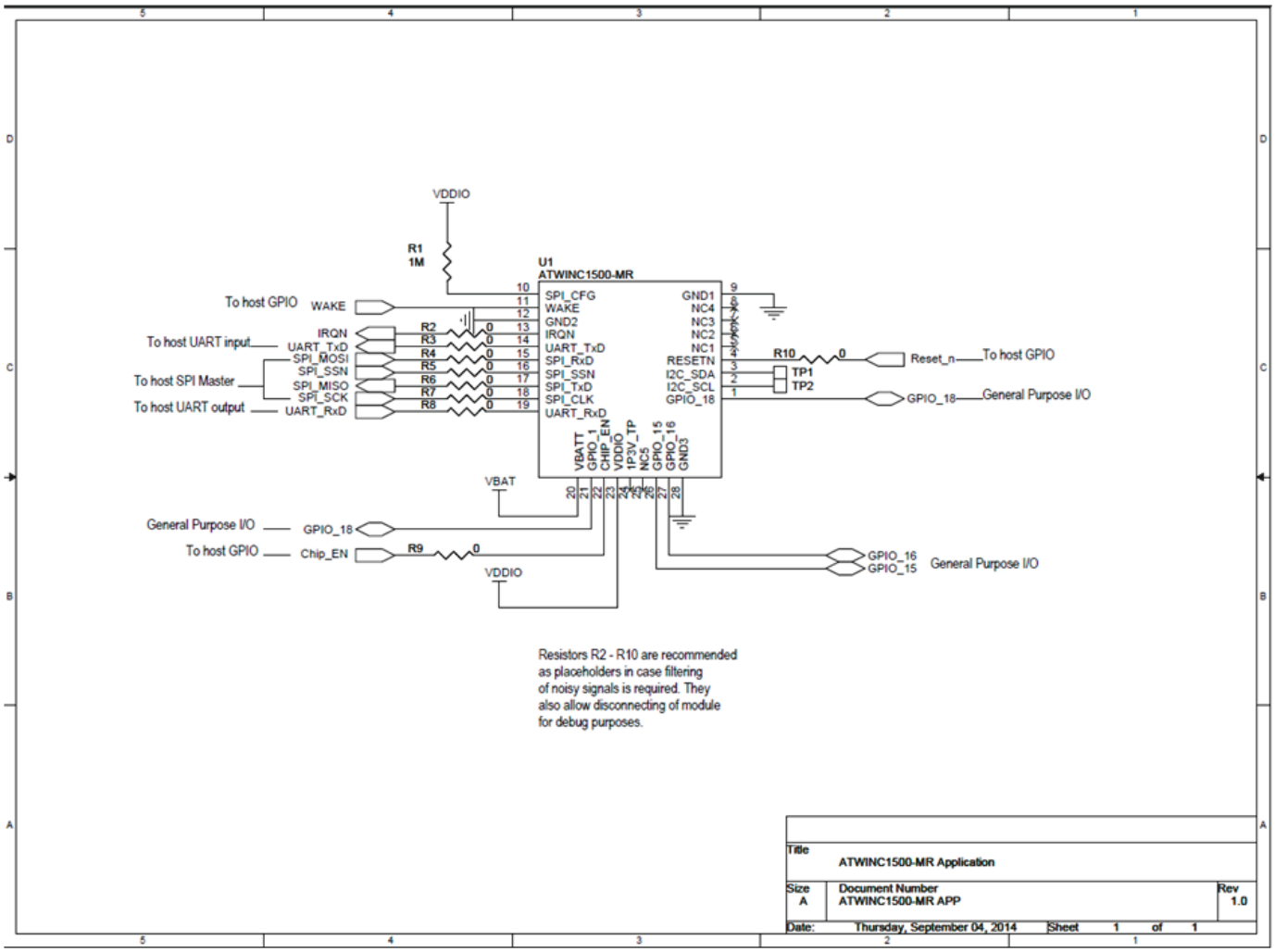
ATWINC1500-MR210P Revision: A

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	2	C5,C12	1.0uF	CAP,CER,1.0uF,20%,X5R,0402,6.3V	Panasonic	ECJ-0EB0J105M	CS0402
2	2	C1,C14	1000PF	CAP CER 1000PF 50V 10% X7R 0402	Murata	GRM155R71H102KA01D	CS0402
3	7	C2,C3,C4,C8,C9,C10, C11	0.1uF	CAP,CER,0.1uF,10%,X5R,0402,10V	AVX	0402ZD104KAT2A	CS0402
4	1	C13	22pF	CAP,CER,22pF,5%,NPO,0402,50V	Murata	GRM1555C1H220JZ01	CS0402
5	1	C17	4.7uF	CAP CER 4.7UF 4V 20% X5R 0402	Murata	GRM155R60G475ME47D	CS0402
6	2	C23,C24	1pF	CAP CER 1PF 50V NP0 0201	Murata	GRM0335C1H1R0CA01D	CS0201
7	2	C6,C7	10PF	CAP CER 10PF 50V 1% NP0 0402	Murata	GRM1555C1H100FA01D	CS0402
8	2	C15,C16	1.8PF	CAP CER 1.8PF 50V NP0 0201	Murata	GRM0335C1H1R8CA01D	CS0201
9	1	C19	10uF	CAP CER 10UF 4V 20% X5R 0402	Murata	GRM155R60G106ME44D	CS0402
10	1	C21	0	RES 0.0 OHM 1/20W JUMP 0201 SMD	Panasonic	ERJ-1GN0R00C	RS0201
11	1	C20	1.8PF	CAP CER 1.8PF 50V NP0 0201	Murata	GRM0335C1H1R8CA01D	CS0201
12		C18,C22	DNI				
13	3	FB1,FB2,FB3	BLM15AG121SN1	FERRITE,120 OHM @100MHz,0402	Murata	BLM15AG121SN1	FBS0402
14	1	L1	2.2uH	POWER INDUCTOR,2.2uH,20%,1250mA,0.22ohms,0603	Murata	LQM18PN2R2MFRL	LPS0603
15	2	L2,L5	3.3nH	INDUCTOR 3.3+/-0.2NH 750MA 0201	Murata	LQP03TN3N3C02D	LS0201
16	1	R1	261k	RES 261K OHM 1/10W 1% 0402 SMD	Panasonic	ERJ-2RKF2613X	RS0402
17	1	R2	6.8PF	CAP,CER,6.8pF,NPO,0402,50V	Murata	GRM1555C1H6R8CA01	CS0402
18	1	R3	301k	RES 301K OHM 1/10W 1% 0402 SMD	Panasonic	ERJ-2RKF3013X	RS0402
19		R4	DNI				
20	1	U1	ATWINC1500A-MU	IC, WiFi, 40QFN	Atmel	ATWINC1500A-MU	40QFN
21	1	U2	FT440Aa	1.5MHz, 600mA, Synchronous Step-Down Converter	FMD	FT440Aa	SOT23-5
22	1	U3	NC7SZ66L6X	IC BUS SWITCH SGL SPST 6MICROPAK	Fairchild	NC7SZ66L6X	6-UFDFN
23	1	Y1	26.000MHz	CRYSTAL 26MHZ 10PF SMD	Abracon	ABM10-26.000MHZ-D30-T3	4 SMD
24	1	PCB	-	ATWINC1500-MR210PA	Createk		
25	1	Shield	-	Metal Shield	Createk	NMI RF Shield rev1	

Revision A -Initial release to production.

14. Application Schematic

Figure 14-1. Application Schematic



15. Technical Support and Resources

For technical support and other resources visit: http://www.atmel.com/design-support

16. Revision History

Doc. Rev.	Date	Comments
42376A	10/2014	Initial document release.

Table of Contents

Description 1

Features 1

1. Ordering Information 3
- 1.1 Regulatory certificates 3

2. Block Diagram 4

3. General Specifications 4
- 3.1 Wi-Fi RF Specification 4
- 3.2 Voltages 6

4. Pin Assignments 7
- 4.1 Top View 7
- 4.2 Pin Descriptions 7

5. Host Interfaces 9
- 5.1 I2C Interface 9
- 5.2 SPI Interface 10
- 5.3 UART Interface 12
- 5.4 Host Interface Power-up Sequence Timing Diagram 13

6. VDDIO Load Switch 13

7. Notes On Interfacing To The ATWINC1500-MR210P 14
- 7.1 Programmable Pull Up Resistors 14

8. Recommended Footprint (Unit: mm) 15

9. RF Performance Placement Guidelines 15

10. Recommended Reflow Profile 16

11. Module Outline Drawings 17

12. Module Schematic 18

13. Module Bill of Materials (BOM) 19

14. Application Schematic 20

15. Technical Support and Resources 21

16. Revision History 22

Table of Contents i

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