iMOTION™

High Performance Sensorless Motor Control IC

Description

IRMCK099 is a low cost, high performance OTP memory based motion control ASIC designed primarily for appliance applications. IRMCK099 is designed to implement high performance control solutions for advanced inverterized appliance motor control. IRMCK099 contains the flexible Tiny Motion Control Engine (TinyMCE) for sensorless control of permanent magnet motors over the full speed range. The TinyMCE implements sensorless Field Oriented Control using single or leg shunt current feedback by a combination of hardware and IR-supplied firmware elements. Key components of the complex sensorless control algorithms, such as the Angle Estimator, are provided as complete pre-defined control blocks. The ASIC is designed to eliminate external components and reduce cost by including an A/D converter, analog amplifiers, an overcurrent comparator, watchdog timer and internal oscillator. Strong startup and configuration tools get the motor running quickly without any programming. The user can also create custom control loops and communication protocols for application-specific solutions. A standby power mode can help to increase overall system efficiency. IRMCK099 comes in a 5mmx5mm, 32 pin QFN package.

Features

- TinyMCE (Tiny Motion Control Engine) - Dedicated computation engine for high efficiency sinusoidal sensorless motor control
- Internal Oscillator – no clock required
- Built-in hardware peripheral for single or two shunt current feedback reconstruction and analog circuits
- Supports both interior and surface permanent magnet motor sensorless control
- Loss minimization Space Vector PWM
- Internal ITRIP comparator
- Two-channel analog output (Sigma Delta D/A)
- JTAG programming port for debugging
- UART and I2C serial interface
- Factory Calibrated Analog Inputs
- Capture input
- Watchdog timer with independent internal clock
- Standby low power mode
- Internal 16 Kbyte OTP memory
- CRC Memory Check
- 5V tolerant digital I/O
- 3.3V single supply

Product Summary

Internal clock frequency (SYSCLK)	100MHz
MCE™ computation time	1 SYSCLK
MCE™ computation data range	16 bit signed
OTP Memory	16KB
MCE Data RAM	1.5KB
MCE Program RAM	12KB
FAULT latency (digital filtered)	2 µsec
PWM carrier frequency	1 – 20kHz
A/D input channels	6
A/D converter resolution	12 bits
A/D converter conversion speed	2 µsec
Analog output (PWM) resolution	8 bits
UART baud rate (typ)	57.6 Kbps
Number of digital I/O (max)	8
Package (lead free)	QFN 5x5 32L
Typical 3.3V operating current	< 30mA
Standyby mode power consumption	3.5mW
Integrated Temperature Sensor(typ)	±5degC

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRMCK099M	QFN32	Tape and Reel	3000	IRMCK099MTR
		Tray	2450	IRMCK099M

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1 Overview

IRMCK099 is a new generation International Rectifier integrated circuit device primarily designed as a one-chip solution for inverterized appliance motor control applications. Unlike a traditional microcontroller or DSP, the IRMCK099 provides a built-in closed loop sensorless control algorithm using the unique flexible Tiny Motion Control Engine (TinyMCE) for permanent magnet motors. The MCE™ consists of a collection of control elements, motion peripherals, a dedicated motion control sequencer and internal memory to map internal signal nodes. IRMCK099 also employs a unique single shunt current reconstruction circuit in addition to two leg shunt current sensing circuit to eliminate additional analog/digital circuitry. Integrated op-amps and A/D converter enable a direct shunt resistor interface to the IC. In addition to the built-in Field Oriented Control algorithm, the user can create customized control loops and communication protocols. Four analog inputs and up to nine digital I/O provide resources for application specific functions. Figure 1 shows a typical application schematic using the IRMCK099.

IRMCK099 contains 16 Kbytes of OTP program memory and comes in a compact 5mm x 5mm 32-pin QFN package.

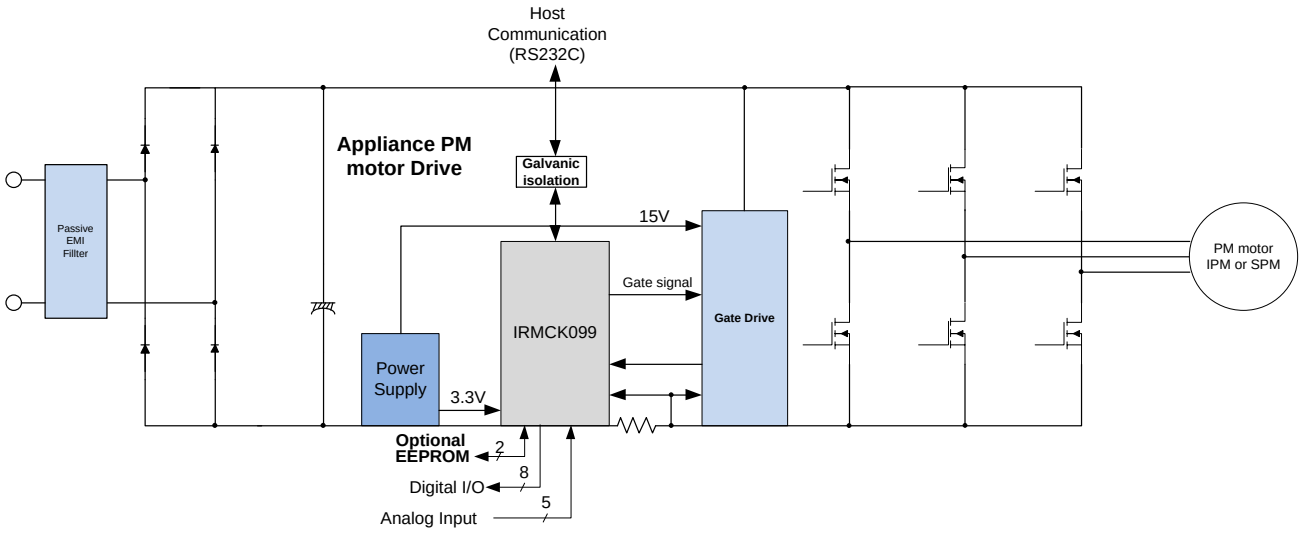


Figure 1. Typical Application Block Diagram Using IRMCK099

2 Pinout

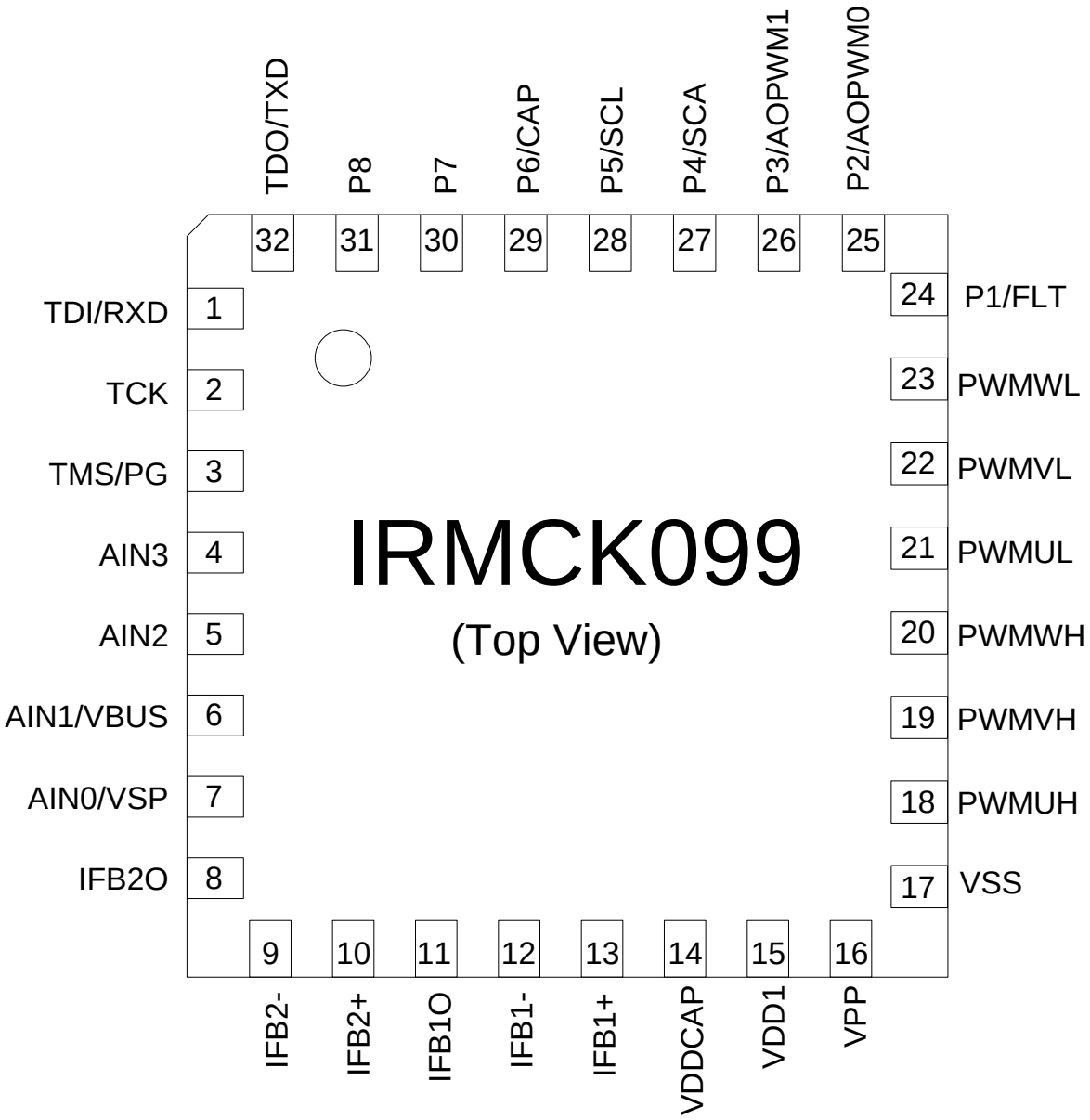


Figure 2. Pinout of IRMCK099

3 IRMCK099 Block Diagram and Main Functions

IRMCK099 block diagram for leg shunt mode is shown in Figure 3.

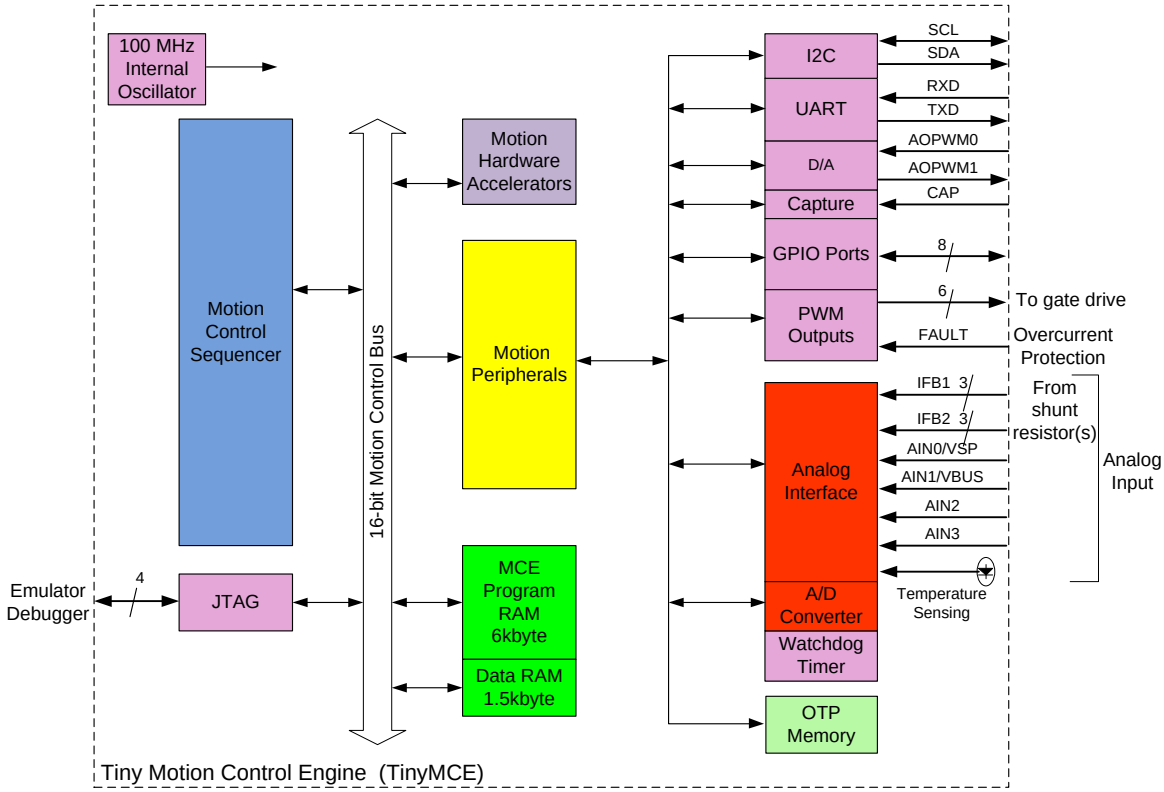


Figure 3. IRMCK099 Block Diagram

IRMCK099 contains the following functions for sensorless permanent magnet motor control applications:

Tiny Motion Control Engine (TinyMCE)

- Sensorless FOC (complete sensorless field oriented control)
  - PI Speed Regulator
  - 2-channel PI Current regulators (q & d quadratures)
  - Angle estimator (sensorless control)
  - Clark/Inverse Clark transformation
  - Vector rotator
  - No parking
  - Torque at low to zero speed
  - Multiply-divide (signed and unsigned)
  - Divide (signed and unsigned)
  - ATAN (arc tangent)
- Hardware PWM shutdown pin (FLT)
- Up to 20kHz PWM Frequency
- One 16 bit watchdog timer
- One 16 bit capture timer
- Up to 8 discrete digital I/Os
- Six-channel 12 bit A/D
  - Buffered (current sensing) two channels (0 – 1.25V input)
  - Unbuffered four channels (0 – 1.25V input)
- JTAG port (4 pins)
- Two channels analog output (8 bit PWM)
- UART
- I^2C port
- Standby Low Power Mode
- 1.5K byte data RAM
- 12K byte program RAM
- 16K byte OTP memory

4 Application connection and Pin function

Figure 4 shows the application connections in leg shunt mode.

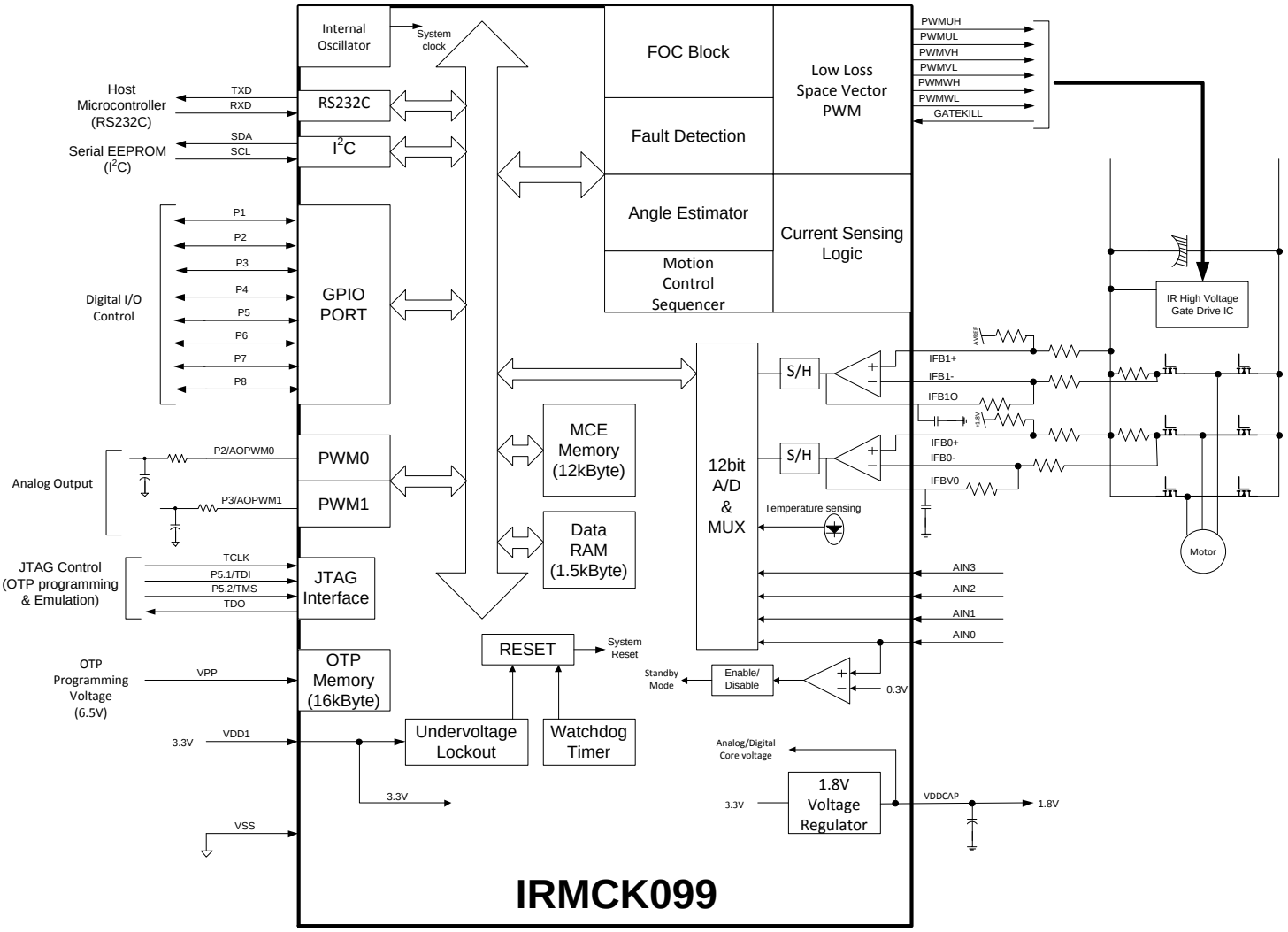


Figure 4. IRMCK099 Leg Shunt Connection Diagram

4.1 MCE Peripheral Interface Group

UART Interface

TXD	Output, Transmit data from IRMCK099, can be configured to GPIO pins
RXD	Input, Receive data to IRMCK099, can be configured to GPIO pins

Discrete I/O Interface

P1	Input/output port 1, pulled up by 49kOhm internal resistor
P2	Input/output port 2

P3	Input/output port 3
P4	Input/output port 4
P5	Input/output port 5
P6	Input/output port 6
P7	Input/output port 7
P8	Input/output port 8

Analog Output Interface

AOPWM1	Input/output, can be configured as 8-bit PWM output 1 with programmable carrier frequency
AOPWM2	Input/output, can be configured as 8-bit PWM output 2 with programmable carrier frequency

I^2C Interface

SCL	Output, I^2C clock output, can be configured to GPIO pins
SDA	Input/output, I^2C Data line, can be configured to GPIO pins

Capture Interface

CAP	Capture Input, can be configured to GPIO pins

4.2 Motion Peripheral Interface Group

PWM

PWMUH	Output, PWM phase U high side gate signal, tri-state at power up until configured by firmware
PWMUL	Output, PWM phase U low side gate signal, tri-state at power up until configured by firmware
PWMVH	Output, PWM phase V high side gate signal, tri-state at power up until configured by firmware
PWMVL	Output, PWM phase V low side gate signal, tri-state at power up until configured by firmware
PWMWH	Output, PWM phase W high side gate signal, tri-state at power up until configured by firmware
PWMWL	Output, PWM phase W low side gate signal, tri-state at power up until configured by firmware

Fault

FLT	Input, upon assertion this sets all six PWM signals to off state according to setting of active_pol register, pulled up by 49kOhm internal resistor

4.3 Analog Interface Group

IFB1+	Input, Operational amplifier positive input for single or leg shunt resistor current sensing
IFB1-	Input, Operational amplifier negative input for single or leg shunt resistor current sensing
IFB1O	Output, Operational amplifier output for single or leg shunt resistor current sensing
IFB2+	Input, Operational amplifier positive input for 2^{nd} leg shunt resistor current sensing
IFB2-	Input, Operational amplifier negative input for 2^{nd} leg shunt resistor current sensing
IFB2O	Output, Operational amplifier output for 2^{nd} leg shunt resistor current sensing
AIN0/VSP	Input, Analog input channel 0 (0 – 1.25 V), also used for Standby Mode wake-up

AIN1/VBUS	Input, Analog input channel 1 (0 – 1.25 V), typically configured for DC bus voltage input
AIN2	Input, Analog input channel 2 (0 – 1.25 V), needs to be pulled down to VSS if unused
AIN3	Input, Analog input channel 3 (0 – 1.25 V), needs to be pulled down to VSS if unused

4.4 Power Interface Group

VDD1	Digital and analog power (3.3V)
VDDCAP	Internal 1.8V output, requires capacitors to the pin. **Note:** The internal 1.8V supply is not designed to power any external circuits or devices. Only capacitors should be connected to this pin.
VSS	Digital and Analog common

4.5 Test Interface Group

TMS	JTAG test mode input or input digital port
TDO	JTAG data output
TDI	JTAG data input, or input digital port
TCK	JTAG test clock

5 DC Characteristics

5.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Condition
V_{DD1}	Supply Voltage	-0.3 V	-	3.6 V	Respect to VSS
V_{IA}	Analog Input Voltage	-0.3 V	-	1.98 V	Respect to VSS
V_{ID}	Digital Input Voltage	-0.3 V	-	3.6 V	Respect to VSS
T_A	Ambient Temperature	-40 ˚C	-	125 ˚C	
T_S	Storage Temperature	-65 ˚C	-	150 ˚C	

Table 1. Absolute Maximum Ratings

Caution: Stresses beyond those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

5.2 System Clock Frequency and Power Consumption

VDD1=3.3V, Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
SYSCLK	System Clock	-	100	-	**MHz**
P_D	Power Consumption		100[1)]	-	**mW**
P_{STBY}	Standby Power Consumption		3.5		**mW**

Table 2. System Clock Frequency

Note 1) The value is based on the condition of MCE clock=100MHz with an actual motor running by a typical TinyMCE application program.

5.3 Digital I/O DC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
V_{DD1}	Supply Voltage	3.0 V	3.3 V	3.6 V	Recommended
V_{IL}	Input Low Voltage	-	-	0.8 V	Recommended
V_{IH}	Input High Voltage	2.0 V		-	Recommended
C_{IN}	Input capacitance	-	1.6 pF	-	(1)
I_L	Input leakage current		±10 nA	±1 µA	V_O = 3.3 V or 0 V
I_{OL}	Low level output current	14.1mA	22.9mA	31.8mA	V_{OL} = 0.4 V (1)
I_{OH}	High level output current	21.8mA	44.2mA	73.5mA	V_{OH} = 2.4 V (1)

Table 3. Digital I/O DC Characteristics

Note:

(1) Data guaranteed by design.

5.4 Analog I/O DC Characteristics

- OP amps for current sensing (IFB1+,IFB1-,IFB1O, IFB2+,IFB2-,IFB2O)

VDD1=3.3V, Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
V_{OFFSET}	Input Offset Voltage	-20mV	3mV	20mV	V_{VDD1} = 3.3 V
V_I	Input Voltage Range	0 V		1.2 V	Recommended
V_{OUTSW}	OP amp output operating range	50 mV (1)	-	1.7 V	V_{VDD1} = 3.3 V
C_{IN}	Input capacitance	-	3.6 pF	-	
R_{FDBK}	OP amp feedback resistor	5 kΩ	-	20 kΩ	Requested between IFBO and IFB-
OP $_{GAINCL}$	Operating Open loop Gain	-	80 db	-	(1)
CMRR	Common Mode Rejection Ratio	-	80 db	-	(1)
I_{SRC}	Op amp output source current	-	1 mA	-	V_{OUT} = 0.6 V
I_{SNK}	Op amp output sink current	-	100 µA	-	V_{OUT} = 0.6 V

Table 4. Analog I/O DC Characteristics

Note:

(1) Data guaranteed by design.

5.5 A/D Accuracy

Unless specified, Ta = 25˚C.

A/D accuracy for current sensing (IFB1+,IFB1-,IFB1O, IFB2+,IFB2-,IFB2O), Vdc (AIN1) sensing and analog input channels (AIN0,AIN2, AIN3)

Symbol	Parameter	Min	Typ	Max	Condition
ADC_{error}	Error is the difference between ideal counts and compensated counts for any applied voltage in 0-1.2V range		±10Counts		(1)

Table 5. A/D Accuracy

Note:

(1) Characterized not tested at manufacturing.

5.6 Under Voltage Lockout DC characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
$UV_{CC3.3+}$	UVcc positive going Threshold	2.55V	2.78V	3.00V	
$UV_{CC3.3-}$	UVcc negative going Threshold	2.40V	2.65V	2.85V	
$UV_{CC3.3}H$	UVcc Hysteresys	-	100mV	-	(1)

Table 5. UVcc 3.3V DC Characteristics

Note:

(1) Data guaranteed by design.

5.7 Itrip comparator DC characteristics

Unless specified, VDD1=3.3V, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
$Itrip_+$	Itrip positive going Threshold	1.2V	1.306V	1.4V	V_{DD1} = 3.3 V
$Itrip_-$	Itrip negative going Threshold	1.05V	1.124V	1.25V	V_{DD1} = 3.3 V
ItripH	Itrip Hysteresys	0.05V	0.182V	0.3V	(1)

Table 6. Itrip DC Characteristics

Note:

(1) Data guaranteed by design.

5.8 Wake-up threshold DC characteristics

Unless specified, VDD1=3.3V, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
V_{WK}	Exit from Standby Threshold	0.285V	0.315V	0.345V	V_{DD1} = 3.3 V

Table 7. Wake-up threshold DC Characteristics

5.9 Integrated Temperature Sensor

Unless specified, VDD1=3.3V

Symbol	Parameter	Min	Typ	Max	Condition
T_{sense}	Integrated T_{sense} Error	-	±5˚C	-	V_{DD1} = 3.3 V Ta = - 40˚C, 25˚C, 125˚C

Table 8. Wake-up threshold DC Characteristics

6 AC Characteristics

6.1 Internal Oscillator AC Characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
F_{CLK}	Clock Frequency	99MHz	100MHz	101MHz	VDD1 = 3.3V

Table 8. Internal Oscillator AC Characteristics

6.2 Analog to Digital Converter AC Characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
T_{CONV}	Conversion time	-	-	2.05 µsec	(1)
T_{HOLD}	Sample/Hold maximum hold time	-	-	10 µsec	Voltage droop ≤ 15 LSB (see figure below)

Table 9.A/D Converter AC Characteristics

Note:

(1) Data guaranteed by design.

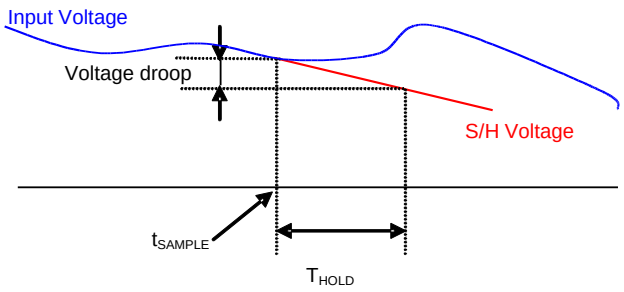


Figure 5. Voltage droop and S/H hold time

6.3 Op amp AC Characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
OP_{SR}	OP amp slew rate	-	10 V/µsec	-	VDD1 = 3.3 V, CL = 33 pF (1)
OP_{IMP}	OP input impedance	-	10^8 Ω	-	(1) (2)
T_{SET}	Settling time	-	400 ns	-	VDD1 = 3.3 V, CL = 33 pF (1)

Table 10 Current Sensing OP Amp AC Characteristics

Note:

(1) Data guaranteed by design.

(2) To guarantee stability of the operational amplifier, it is recommended to load the output pin by a capacitor of 47pF, see Figure 6. Here only the single shunt current amplifier is shown but all op amp outputs should be loaded with this capacitor value.

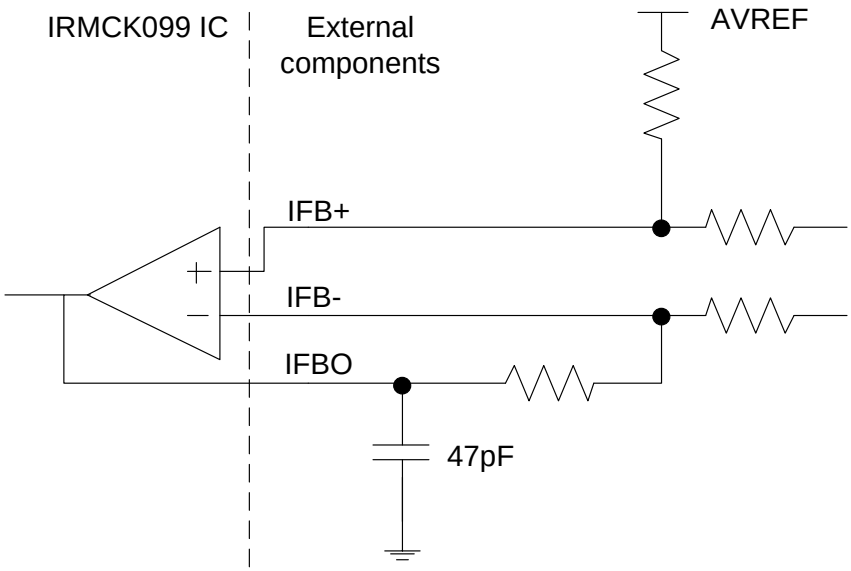


Figure 6. Op amp output capacitor

6.4 SYNC to SVPWM and A/D Conversion AC Timing

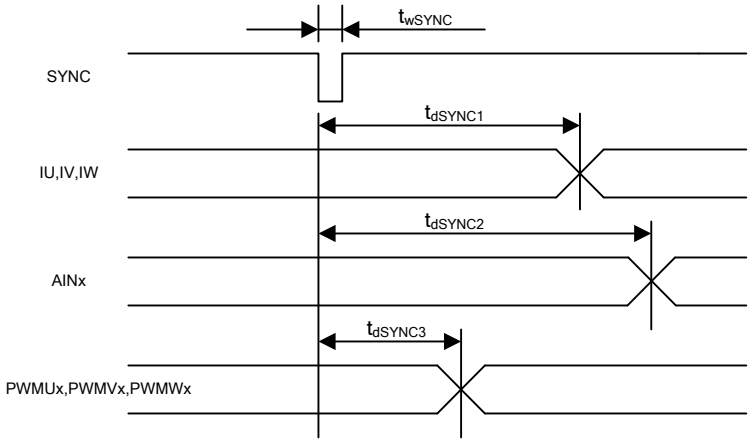


Figure 7. SYNC timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wSYNC}	SYNC pulse width	-	32	-	SYSCLK
t_{dSYNC1}	SYNC to current feedback conversion time	-	-	100	SYSCLK
t_{dSYNC2}	SYNC to AIN0-4, ADCH, ADCL analog input conversion time	-	-	200	SYSCLK (1)
t_{dSYNC3}	SYNC to PWM output delay time	-	-	2	SYSCLK

Table 11. SYNC AC Characteristics

Note:

(1) AIN1 – AIN5 channels are converted once every 5 SYNC events

6.5 FAULT to SVPWM AC Timing

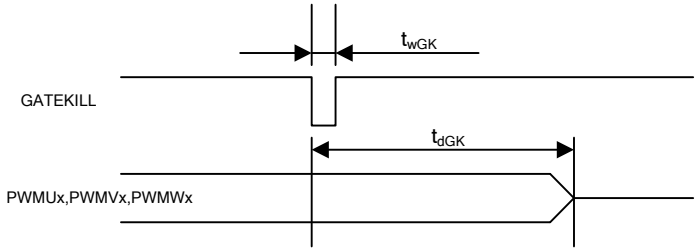


Figure 8. Fault timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wGK}	FAULT pulse width	32	-	-	SYSCLK
t_{dGK}	FAULT to PWM output delay	-	-	100	SYSCLK

Table 12. FAULT to SVPWM AC Timing

6.6 ITRIP AC Timing

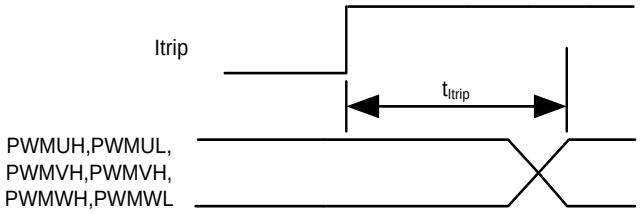


Figure 9. ITRIP timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{ITRIP}	Itrip propagation delay	-	-	100(sysclk)+1.0usec	SYSCLK+usec

Table 13. Itrip AC Timing

6.7 I²C AC Timing

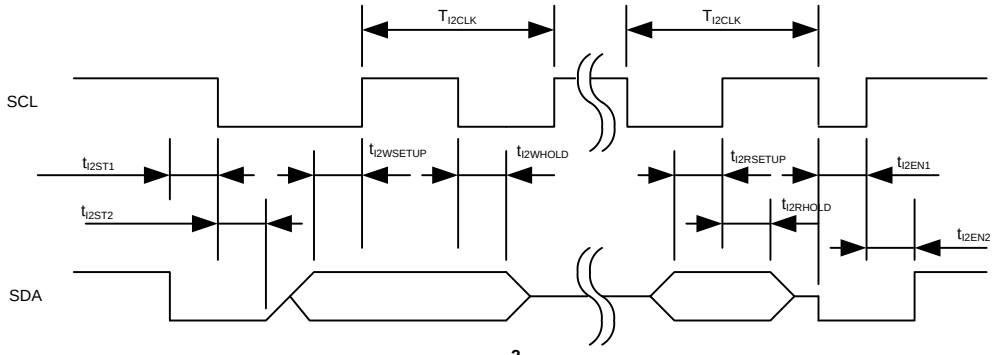


Figure 10. I²C Timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{I2CLK}	I²C clock period	10	-	8192	SYSCLK
t_{I2ST1}	I²C SDA start time	0.25	-	-	T_{I2CLK}
t_{I2ST2}	I²C SCL start time	0.25	-	-	T_{I2CLK}
$t_{I2WSETUP}$	I²C write setup time	0.25	-	-	T_{I2CLK}
$t_{I2WHOLD}$	I²C write hold time	0.25	-	-	T_{I2CLK}
$t_{I2RSETUP}$	I²C read setup time	I²C filter time(1)	-	-	SYSCLK
$t_{I2RHOLD}$	I²C read hold time	1	-	-	SYSCLK

Table 14. I²C AC Timing

Note:

(1) I²C read setup time is determined by the programmable filter time applied to I²C communication.

6.8 UART AC Timing

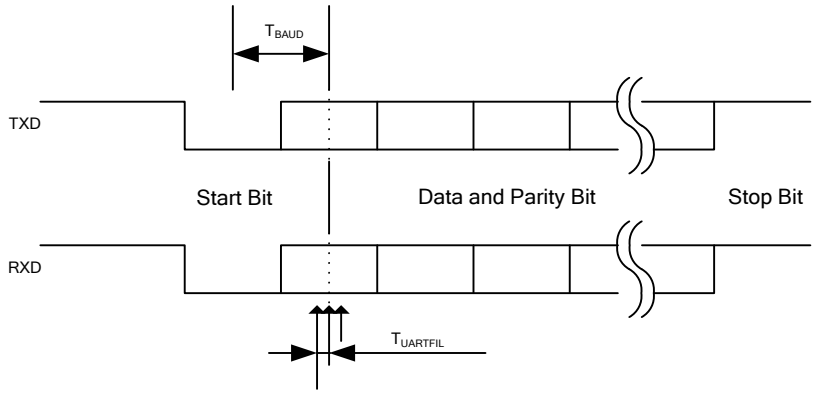


Figure 11. UART timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{BAUD}	Baud Rate Period	-	57600	-	bit/sec
$T_{UARTFIL}$	UART sampling filter period (1)	-	1/16	-	T_{BAUD}

Table 15. UART AC Timing

Note:

(1) Each bit including start and stop bit is sampled three times at center of a bit at an interval of 1/16 T_{BAUD}. If three sampled values do not agree, then UART noise error is generated.

6.9 CAPTURE Input AC Timing

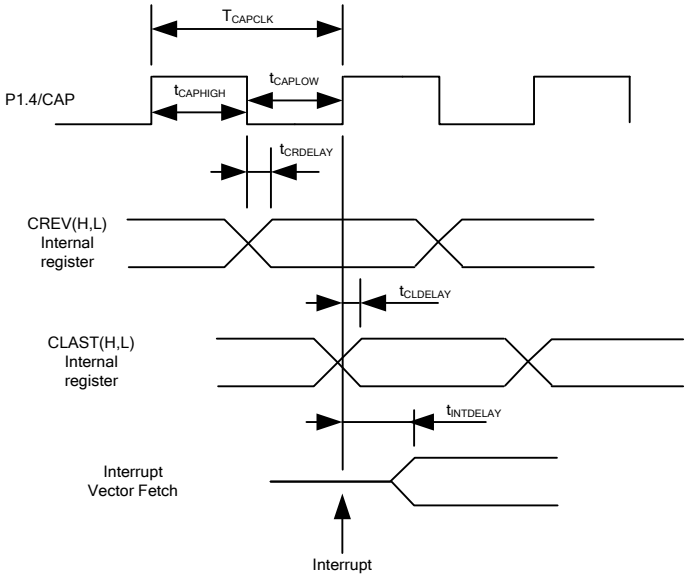


Figure 12. CAPTURE timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{CAPCLK}	CAPTURE input period	8	-	-	SYSCLK
$t_{CAPHIGH}$	CAPTURE input high time	4	-	-	SYSCLK
t_{CAPLOW}	CAPTURE input low time	4	-	-	SYSCLK
$t_{CRDELAY}$	CAPTURE falling edge to capture register latch time	-	-	4	SYSCLK
$t_{CLDELAY}$	CAPTURE rising edge to capture register latch time	-	-	4	SYSCLK
$t_{INTDELAY}$	CAPTURE input interrupt latency time	-	-	4	SYSCLK

Table 16. CAPTURE AC Timing

6.10 JTAG AC Timing

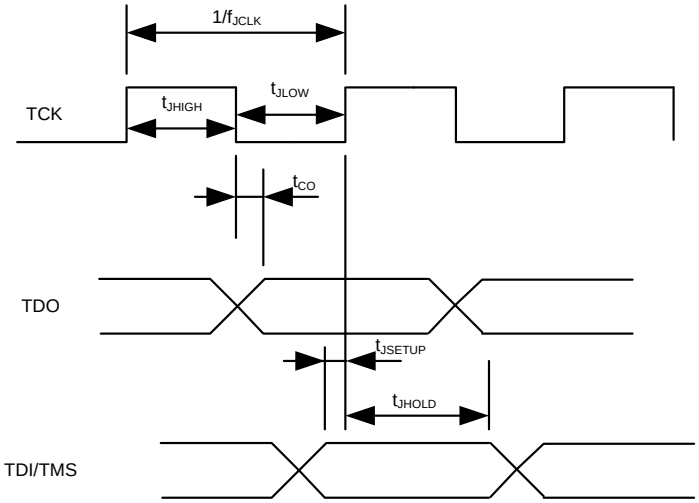


Figure 13. JTAG timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
f_{JCLK}	TCK Frequency	-	-	10	MHz
t_{JHIGH}	TCK High Period	10	-	-	nsec
t_{JLOW}	TCK Low Period	10	-	-	nsec
t_{CO}	TCK to TDO propagation delay time	0	-	5	nsec
t_{JSETUP}	TDI/TMS setup time	4	-	-	nsec
t_{JHOLD}	TDI/TMS hold time	0	-	-	nsec

Table 17. JTAG AC Timing

7 I/O Structure

The following figure shows the I/O structure for all digital pins. At power up, the programmable pull up transistor is off.

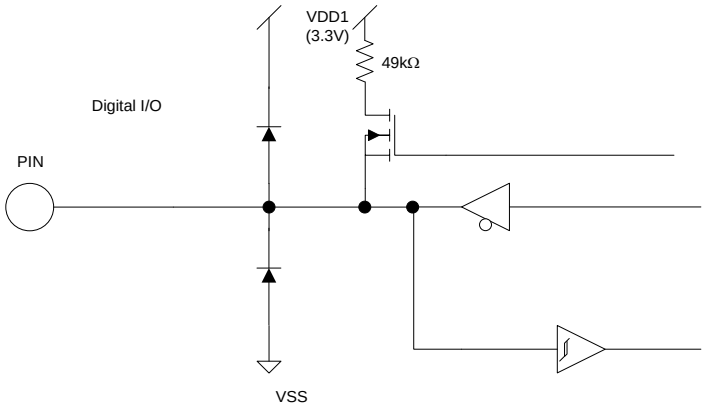


Figure 14. Digital I/O Structure

The following figure shows the analog input/output structure, except for AIN0/STBY.

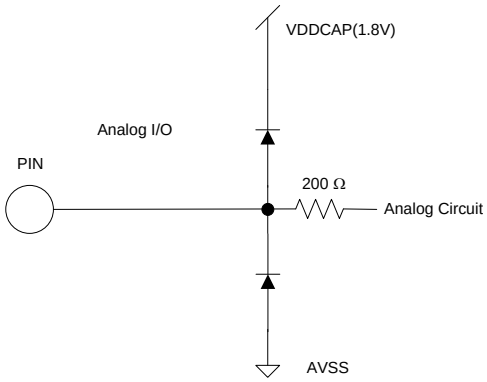


Figure 15. Analog I/O Structure

The following figure shows all the input structure for AIN0/STBY pin.

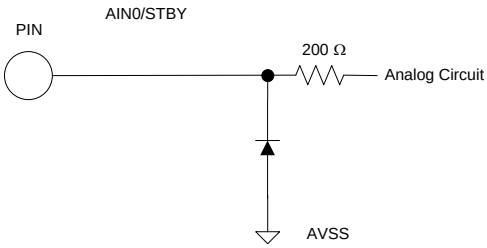


Figure 16 Analog Analog Input Structure for AIN0/STBY

The following figure shows the VSS pin I/O structure

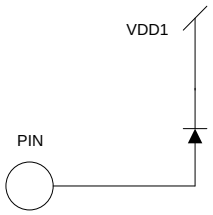


Figure 17. VSS pin I/O structure

The following figure shows the,VDDCAP pin I/O structure

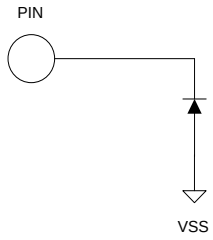


Figure 18. VDDCAP pin I/O structure

The following figure shows the,VDD1 pin I/O structure

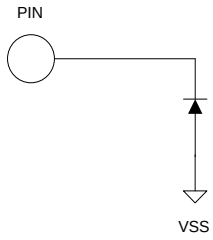


Figure 19. VDD1 pin I/O structure

8 Pin List

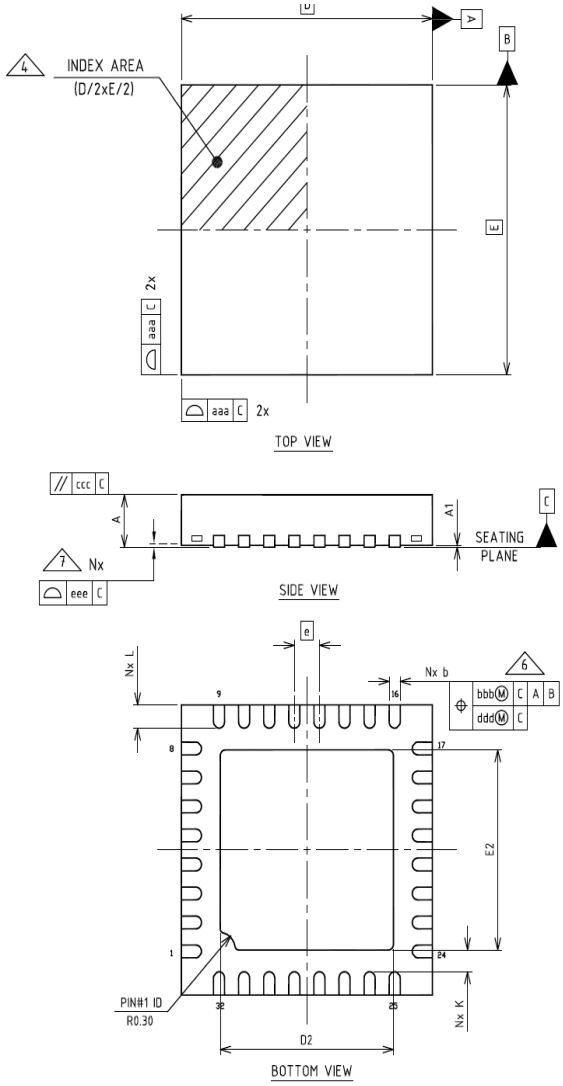
Pin Number	Pin Name	Internal Pull-up	Pin Type	Description
1	TDI/RXD	49 KΩ pull up(1)	I	JTAG test data input or UART receiver input
2	TCK	49 KΩ pull up(1)	I	JTAG test clock
3	TMS/PG	49 KΩ pull up(1)	I/O	JTAG test mode input or Discrete programmable I/O
4	AIN3		I	Analog input channel 3, 0-1.25V range, needs to be pulled down to VSS if unused
5	AIN2		I	Analog input channel 2, 0-1.25V range, needs to be pulled down to VSS if unused
6	AIN1/VBUS		I	Analog input channel 1, 0-1.25V range, used for DC Bus Voltage Input
7	AIN0/STBY		I	Analog input channel 0, 0-1.25V range, exit standby if >300mV
8	IFB2O		O	Operational amplifier output for 2nd leg shunt resistor current sensing
9	IFB2-		I	Operational amplifier negative input for 2nd leg shunt resistor current sensing
10	IFB2+		I	Operational amplifier positive input for 2nd leg shunt resistor current sensing
11	IFB1O		O	Operational amplifier output for single or leg shunt resistor current sensing
12	IFB1-		I	Operational amplifier negative input for single or leg shunt resistor current sensing
13	IFB1+		I	Operational amplifier positive input for single or leg shunt resistor current sensing
14	VDDCAP		P	Internal 1.8V output, Capacitor(s) to be connected
15	VDD1		P	3.3V digital and analog power
16	VPP		P	OTP Programming voltage (6.75V)
17	VSS		P	Digital common
18	PWMUH	49 KΩ pull up(1)	O	PWM gate drive for phase U high side, configurable either high or low true
19	PWMVH	49 KΩ pull up(1)	O	PWM gate drive for phase V high side, configurable either high or low true
20	PWMWH	49 KΩ pull up(1)	O	PWM gate drive for phase W high side, configurable either high or low true
21	PWMUL	49 KΩ pull up(1)	O	PWM gate drive for phase U low side, configurable either high or low true
22	PWMVL	49 KΩ pull up(1)	O	PWM gate drive for phase V low side, configurable either high or low true
23	PWMWL	49 KΩ pull up(1)	O	PWM gate drive for phase W low side, configurable either high or low true.
24	P1/FLT	49 KΩ pull up(1)	I/O	PWM shutdown input, configurable digital filter, active low input or Discrete programmable I/O
25	P2/AOPWM0	49 KΩ pull up(1)	I/O	Discrete programmable I/O or D/A Output
26	P3/AOPWM1	49 KΩ pull up(1)	I/O	Discrete programmable I/O or D/A Output
27	P4/SCA	49 KΩ pull up(1)	I/O	Discrete programmable I/O or I2C Data
28	P5/SCL	49 KΩ pull up(1)	I/O	Discrete programmable I/O or I2C Clock Output
29	P6	49 KΩ pull up(1)	I/O	Discrete programmable I/O
30	P7	49 KΩ pull up(1)	I/O	Discrete programmable I/O

Pin Number	Pin Name	Internal Pull-up	Pin Type	Description
31	P8	49 KΩ pull up(1)	I/O	Discrete programmable I/O
32	TDO/TXD	49 KΩ pull up(1)	O	JTAG test data output or UART transmitter output

Table 18. Pin List

(1) Programmable internal pull up

9 Package Dimensions

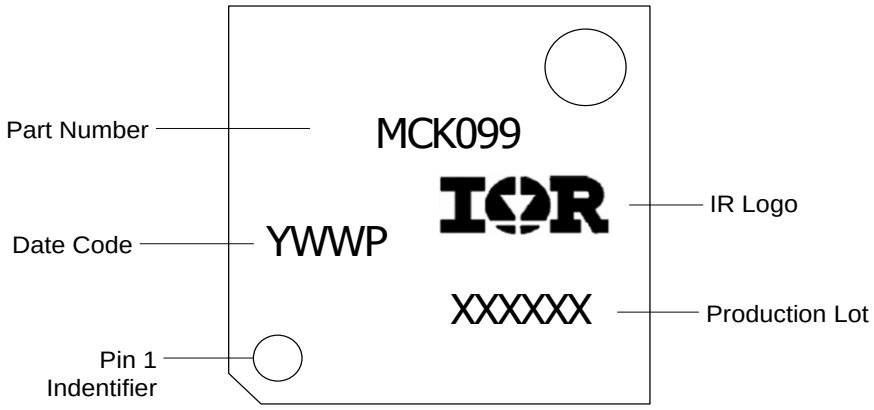


Dimension Table				
Thickness / Symbol	W : Very Very Thin			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
b	0.18	0.25	0.30	6
D		5.00 BSC		
E		5.00 BSC		
e		0.50 BSC		
D2	3.30	3.45	3.55	
E2	3.30	3.45	3.55	
K	0.20	---	---	
L	0.30	0.40	0.50	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		32		3
ND		8		5
NE		8		5
NOTES		1, 2		
LF PART NO.		437727		
LF DWG. NO.		CARSEM-06257		
REV.		A		

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals on D and E side repectively .
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization.

10 Part Marking Information



11 Qualification Information

Qualification Level		Industrial[††] (per JEDEC JESD47)
Moisture Sensitivity Level		MSL2[†††] (per IPC/JEDEC J-STD-020)
ESD	**Machine Model**	Class B (per JEDEC standard JESD22-A115)
	Human Body Model	Class 2 (per ANSI/ESDA/JEDEC JS-001)
	Charged Device Model	Class C2 (per JEDEC standard JESD22-C101)
	Latch-Up	Class I, Level B (per JEDEC standard JESD78)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Revision History

Rev A (March 18, 2014)	First Revision

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