Design Example Report

Title	***1.5 W Non-Isolated Flyback Power Supply with 0.00 W Power Down Mode Using LinkZero^{TM}-AX LNK584DG***
Specification	85 VAC – 265 VAC Input; 5 V, 300 mA Output
Application	LinkZero-AX Reference Design
Author	Applications Engineering Department
Document Number	DER-260
Date	October 13, 2010
Revision	1.3

Summary and Features

- Non-isolated design provides tight regulation.
- Low cost, low component count solution
- Power Down (PD) Mode set and reset functionality. Less than 5 mW no load consumption at 230 VAC (IEC62301 Clause 4.5 rounds standby power use below 5 mW to zero)
- Auto-restart functionality provides protection against output short circuit and open loop conditions
- Hysteretic over temperature shutdown protection
- Meets EN-550022 and CISPR-22 Class B conducted EMI with more than 10 dB margin.
- Meets IEC61000-4-5 Class 3 AC line surge specifications

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5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This report describes a universal input, 5 V, 300 mA non-isolated flyback power supply which is designed with LNK584DG device from the LinkZero-AX family of ICs. It contains the complete specification of the power supply, a detailed circuit diagram, the entire bill of materials required to build the supply, extensive documentation of the power transformer, along with test data and oscillographs of the most important electrical waveforms.



Figure 1 – Prototype Top View.

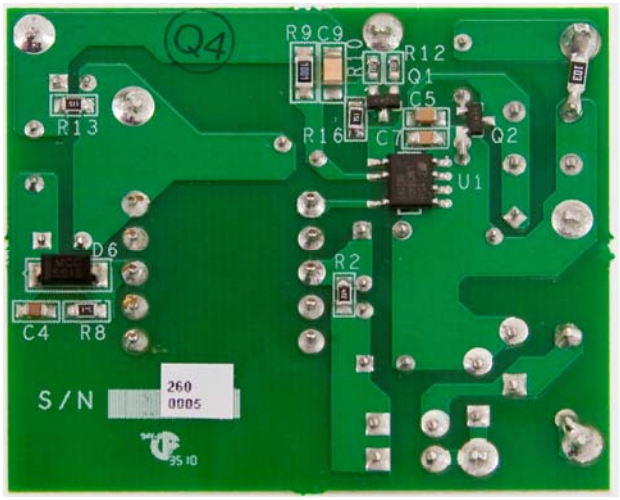


Figure 2 – Prototype Bottom View.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power					mW	230 VAC
Output						
Output Voltage	V_{OUT}		5		V	See V-I Curves for limits
Output Ripple Voltage	V_{RIPPLE}			50	mV	20 MHz bandwidth
Output Current	I_{OUT}			300	mA	
Total Output Power						
Continuous Output Power	P_{OUT}			1.5	W	
Efficiency						
Full load efficiency	η		67		%	
Environmental						
Conducted EMI		Meets CISPR22B / EN55015B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge	DM	1			kV	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
	CM	2				
Ambient Temperature	T_{AMB}	0		50	°C	Free convection, sea level

3 Schematic

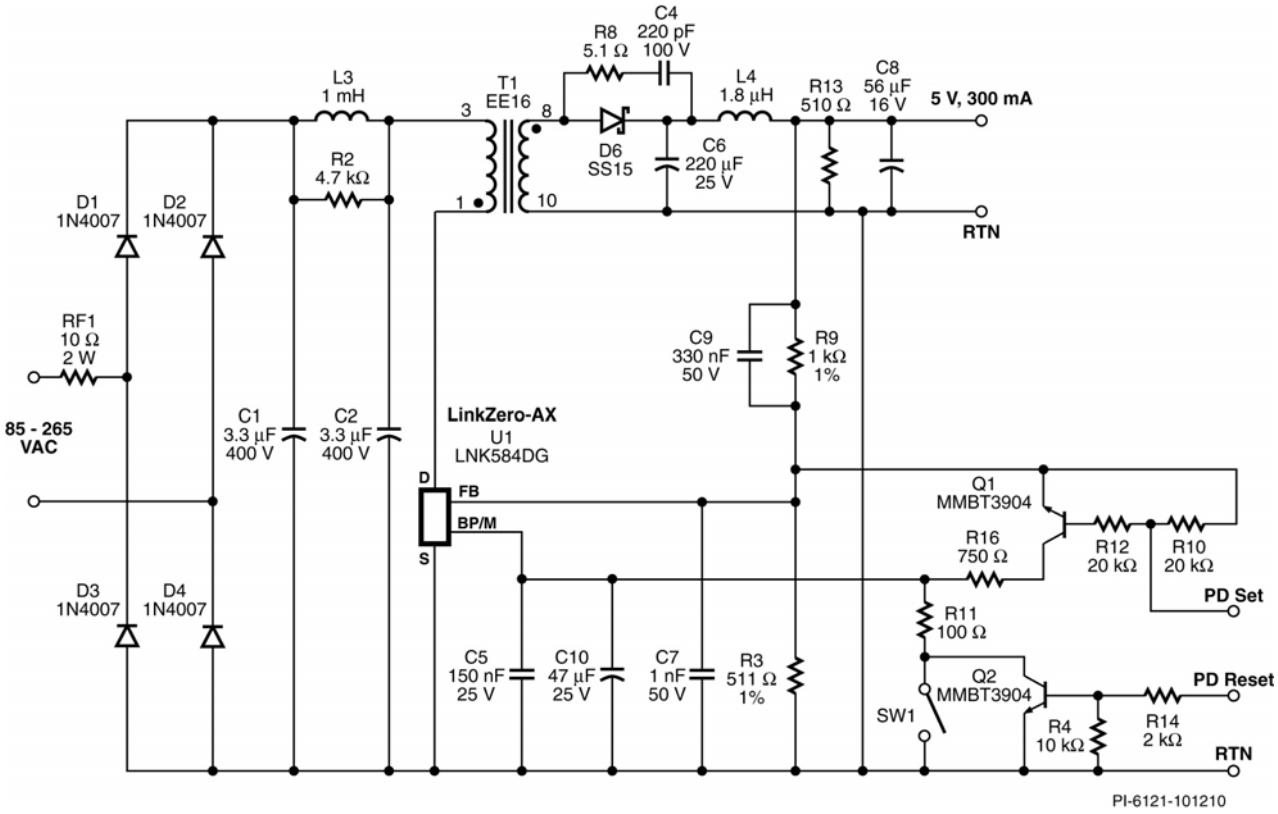


Figure 3 – Circuit Schematic.

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4 Circuit Description

4.1 Input Rectification and Filtering

Diodes D1 to D4 rectify the AC input which is filtered by C1 and C2. Inductor L3, C1 and C2 form a π filter that attenuates differential mode conducted EMI. Resistor R2 provides high frequency damping. Shielding techniques (*E-Shield*™) were used in the construction of T1 to reduce common mode EMI displacement currents. This filter arrangement, the proprietary E-Shield techniques together with IC's frequency jitter function provide excellent EMI performance for this solution even without a Y capacitor or a primary-side RCD clamp circuit.

4.2 LinkZero-AX Primary

The LNK584DG device (U1) integrates an oscillator, an ON/OFF controller, startup and protection circuitry and a power MOSFET all on one monolithic IC.

One side of the power transformer is connected to the positive leg of C2 and the other side is connected to the DRAIN pin of U1. At the start of a switching cycle, the controller turns the MOSFET on, and current ramps up in the primary winding, which stores energy in the core of the transformer. When that current reaches the limit threshold, the controller turns the MOSFET off. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy then induces a voltage across the secondary winding, which forward biases the output diode, and the stored energy is delivered to the output capacitor.

4.3 Primary Clamp and Transformer Construction

A *Clampless* primary circuit is achieved due to the very tight tolerance current limit trimming techniques used in manufacturing the LNK584DG, together with some special transformer construction techniques that were used. Peak drain voltage is therefore limited to typically less than 550 V at 265 VAC – providing significant margin to the 700 V drain voltage (BV_{DSS}).

4.4 Output Rectification

Output rectification is provided by diode D6 and filtering is provided by capacitor C6. Resistor R8 and C4 provide high frequency filtering for improved EMI.

4.5 Power Down (PD) Mode – Set and Reset

LinkZero-AX goes into Power Down mode when one of the following two conditions have been met:

(i) 160 consecutive cycles have been skipped.
(ii) FB voltage exceeds 1.7 V for 160 consecutive switching cycles (approximately 2 ms).

The latter condition is the preferred way of setting the supply into "Power Down" (PD) mode. In this circuit the FB pin is pulled high through Q1 and R16. The value of the BP pin capacitor should be high enough to sustain enough current through R16 for more

than 2 ms to successfully trigger the Power Down mode. LinkZero-AX stops switching once the power down mode is triggered (PD set), and the chip cannot wake up (PD reset) until the BP pin capacitor is pulled below 1.5 V and then released to be recharged. Transistor Q2 or the mechanical switch SW1 can be used to reset the Power Down mode.

Load transients from full load to very light or no load can cause accidental triggering of the Power Down mode. To avoid this undesired effect, a preload must be used at the output of the power supply. Additionally, a capacitor (C9) in parallel to the high side feedback resistor (R9) can be used to speed up the high frequency loop response. Low value feedback resistors can act as preload too. For applications with limited load range, which guarantee that accidental power down mode will not be triggered, the preload and the capacitor in parallel to the high side feedback resistor are not necessary.

4.6 Feedback

The output voltage is sensed through resistor divider R3 and R9 and fed back to U1. Switching cycles are skipped if the FB pin disable threshold voltage (1.7 V) is exceeded. When the sensed voltage at the FB pin falls below the disable threshold, switching cycles are re-enabled. By adjusting the ratio of enabled to disable switching cycles, output regulation is maintained.

At increased loads, beyond the output power limiting point, the FB pin voltage begins to reduce as the power supply output voltage falls. As the FB pin voltage falls, the switching frequency reduces to provide some output current limiting. When the FB pin voltage drops below the auto-restart threshold (typically 0.9 V on the FB pin), the power supply enters the auto-restart mode. In this mode, the power supply will turn off for 1.2 s and then turn back on for 170 ms. The auto-restart function reduces the average output current during an output short-circuit condition.

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5 PCB Layout

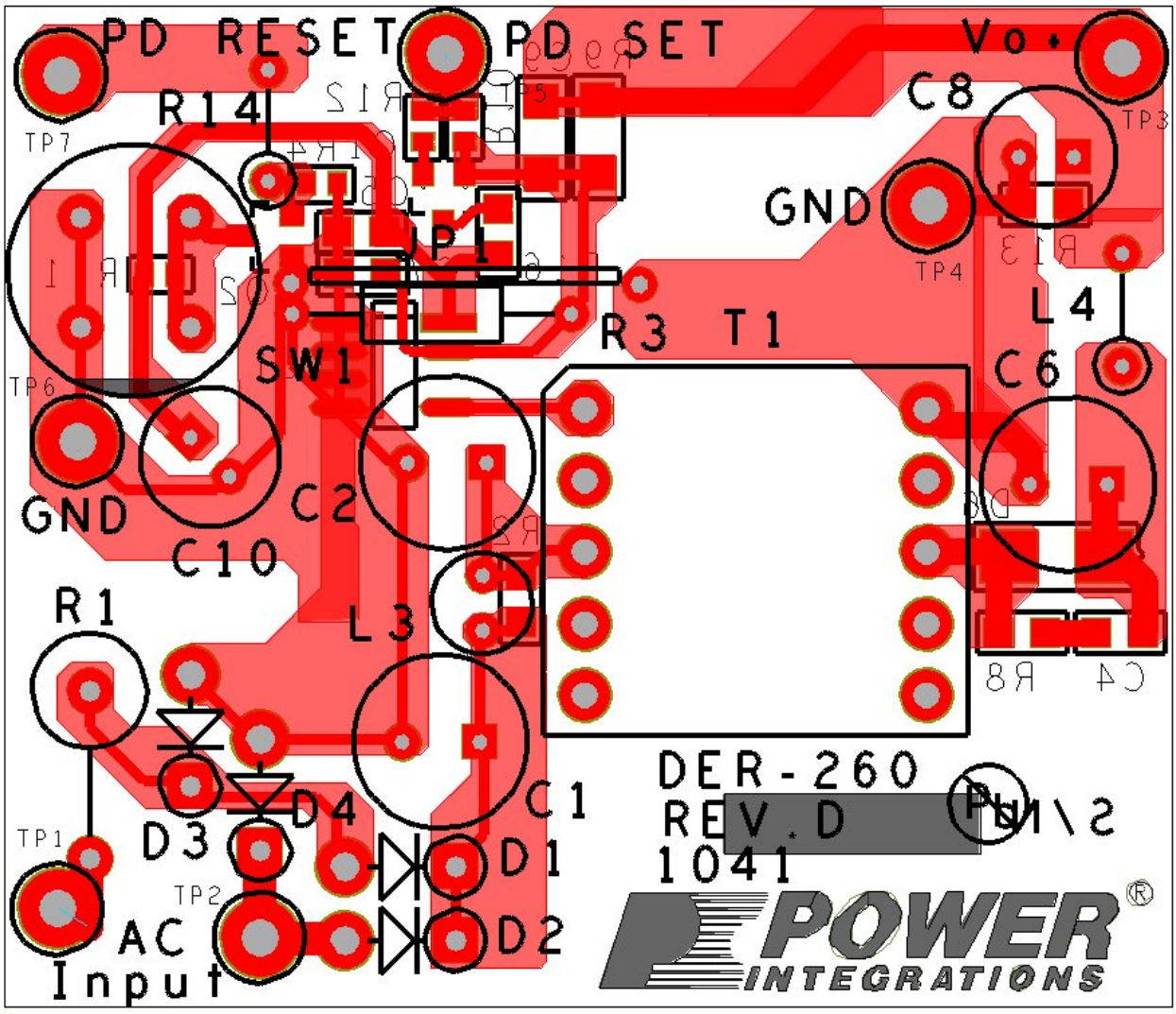


Figure 4 – PCB Layout 2.10” (53.3 mm) x 1.81” (46.1 mm)

6 Bill of Materials

Item	Qty	Ref Des	Description	Manufacturer P/N	Manufacturer
1	1	C1	3.3 μF, 400 V, Electrolytic, (8 x 11.5)	TAQ2G3R3MK0811MLL3	Taicon Corporation
2	1	C2	3.3 μF, 400 V, Electrolytic, (8 x 11.5)	TAQ2G3R3MK0811MLL3	Taicon Corporation
3	1	C4	220 pF, 100 V, Ceramic, X7R, 0805	ECJ-2VB2A221K	Panasonic
4	1	C5	150 nF, 25 V, Ceramic, X7R, 0805	GRM21BR71E154KA01L	Murata
5	1	C6	220 μF, 25 V, Electrolytic, Very Low ESR, 72 mΩ, (8 x 11.5)	EKZE250ELL221MHB5D	Nippon Chemi-Con
6	1	C7	1 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H102K	Panasonic
7	1	C8	56 μF, 16 V, Electrolytic, Gen. Purpose, (5 x 11)	EKZE160ELL560ME11D	Nichicon
8	1	C9	330 nF, 50 V, Ceramic, X7R, 1206	12065C334KAT2A	AVX Corp
9	1	C10	47 μF, 25 V, Electrolytic, Very Low ESR, 300 mΩ, (5 x 11)	EKZE250ELL470ME11D	Nippon Chemi-Con
10	1	D1	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
11	1	D2	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
12	1	D3	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
12	1	D4	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
14	1	D6	50 V, 1 A, Schottky, DO-214AC	SS15-TP	Micro commercial
15	1	L3	1 mH, 0.15 A, Ferrite Core	SBCP-47HY102B	Tokin
16	1	L4	1.8 μH, 0.48 A, Iron Core	1025-26K	API Delevan
17	1	Q1	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-23	MMBT3904LT1G	On Semiconductor
18	1	Q2	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-23	MMBT3904LT1G	On Semiconductor
19	1	R1	10 Ω, 2 W, Fusible/Flame Proof Wire Wound	CRF253-4 10R	Vitrohm
20	1	R2	4.7 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ472V	Panasonic
21	1	R3	511 Ω, 1%, 1/4 W, Metal Film	MFR-25FBF-511R	Yageo
22	1	R4	10.0 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
23	1	R8	5.1 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ5R1V	Panasonic
24	1	R9	1.0 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1001V	Panasonic
25	1	R10	20 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ203V	Panasonic
26	1	R11	100 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
27	1	R12	20 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ203V	Panasonic
28	1	R13	510 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ511V	Panasonic
29	1	R14	2 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-2K0	Yageo
30	1	R16	750 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ751V	Panasonic
31	1	SW1	Pushbutton Switch SPST D6 Series	D6C10LFS	ITT Ind
32	1	T1	Bobbin, EE16, Horizontal, 10 pins	PM-9820	Ho Jinn Plastic Elect
33	1	TP1	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
34	1	TP2	Test Point, BLK ,THRU-HOLE MOUNT	5011	Keystone
35	1	TP3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
36	1	TP4	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
37	1	TP5	Test Point, ORG, THRU-HOLE MOUNT	5013	Keystone
38	1	TP6	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
39	1	TP7	Test Point, YEL, THRU-HOLE MOUNT	5014	Keystone
40	1	U1	LinkZero-AX, LNK584DG, SO-8	LNK584DG	Power Integrations

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7 Transformer Design Spreadsheet

ACDC_LinkZero-AX_082510; Rev.1.1; Copyright Power Integrations 2010	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkZero-AX_082510_Rev1-1.xls; LinkZero-AX Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	5.00			Volts	Output Voltage (main) measured at the end of output cable (For CV/CC designs enter typical CV tolerance limit)
IO	0.30			Amps	Power Supply Output Current (For CV/CC designs enter typical CC tolerance limit)
PO			1.50	Watts	Output Power (VO x IO + dissipation in output cable)
Feedback Type	**Direct**		**Direct**		Choose 'Bias' for Bias winding feedback, 'Direct' for direct sensing of output and 'Opto' for Optocoupler feedback from the 'Feedback Type' drop down box at the top of this spreadsheet
Clampless Design	**Yes**				Choose 'YES' from the 'Clampless Design' drop down box at the top of this spreadsheet for a clampless design. Choose 'NO' to add an external clamp circuit. Clampless design lowers the total cost of the power supply
n	0.65		0.65		Efficiency Estimate at output terminals. For CV only designs enter 0.7 if no better data available
Z			0.5		Loss Allocation Factor (Secondary side losses / Total losses)
tC	2.90			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	6.60			uFarads	Input Capacitance
Input Rectification Type	**F**		**F**		Choose H for Half Wave Rectifier and F for Full Wave Rectification from the 'Rectification' drop down box at the top of this spreadsheet
ENTER LinkZero-AX VARIABLES					
LinkZero-AX	**Auto**		**LNK584**		LinkZero-AX device.
ILIMITMIN			0.126	Amps	Minimum Current Limit
ILIMITMAX			0.146	Amps	Maximum Current Limit
fSmin			93000	Hertz	Minimum Device Switching Frequency. May be lowwer than 93 kHz for high line (230 VAC) designs
I^2fMIN			1664.64	A^2Hz	I^2f Minimum value (product of current limit squared and frequency is trimmed for tighter tolerance)
I^2fTYP			1849.6	A^2Hz	I^2f typical value (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	61.00		61	Volts	Reflected Output Voltage
VDS			10	Volts	LinkZero-AX on-state Drain to Source Voltage
VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
KP			1.58		Ripple to Peak Current Ratio (0.9<KRP<1.0 : 1.0<KDP<6.0)
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EE16**		**EE16**		User-Selected transformer core
Core		EE16		P/N:	PC40EE16-Z
Bobbin		EE16_BOBBIN		P/N:	EE16_BOBBIN
AE			0.192	cm^2	Core Effective Cross Sectional Area
LE			3.5	cm	Core Effective Path Length
AL			1140	nH/T^2	Ungapped Core Effective Inductance
BW			8.6	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			2		Number of primary layers
NS	10.00		10		Number of Secondary Turns
NB			28		Number of Bias winding turns
VB			15.13	Volts	Bias Winding Voltage
R1			1.00	kΩ	Calculated standard value (1%) of Upper Resistor in the resistor divider component between bias winding and FB pin

					of LinkZero-AX
R2			0.51	kΩ	Calculated standard value (1%) of Lower Resistor in the resistor divider component between bias winding and FB pin of LinkZero-AX
RBP			56.00	kΩ	Optional BP pin resistor (connected between BP pin and bias winidng) to improve efficiency. Calculated standard 5% value is displayed
CBIAS (or COUT)			100.00	uF	Maximum value of output capacitor. Larger value may result in issues during startup. Lower value of COUT can be used.
CFB			680.00	pF	FB pin resistor (Improve noise sensitivity)
CBP			220.00	nF	BP pin capacitor
Recommended Bias Diode			1N4003		Place this diode on the return leg of the bias winding for optimal EMI.
DC INPUT VOLTAGE PARAMETERS					
VMIN			97	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.33		Maximum Duty Cycle
IAVG			0.03	Amps	Average Primary Current
IP			0.13	Amps	Minimum Peak Primary Current
IR			0.13	Amps	Primary Ripple Current
IRMS			0.04	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			2287	uHenries	Typical Primary Inductance. +/- 10%
LP_TOLERANCE			10	%	Primary inductance tolerance
NP			111		Primary Winding Number of Turns
ALG			186	nH/T^2	Gapped Core Effective Inductance
BM			1568	Gauss	Maximum Operating Flux Density, BM<2000 is recommended
BAC			784	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1654		Relative Permeability of Ungapped Core
LG			0.12	mm	Gap Length (Lg > 0.08 mm)
BWE			17.2	mm	Effective Bobbin Width
OD			0.16	mm	Maximum Primary Wire Diameter including insulation
INS			0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.12	mm	Bare conductor diameter
AWG			37	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			20	Cmils	Bare conductor effective area in circular mils
CMA			452	Cmils/Amp	Primary Winding Current Capacity (150 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			1.40	Amps	Peak Secondary Current
ISRMS			0.59	Amps	Secondary RMS Current
IRIPPLE			0.51	Amps	Output Capacitor RMS Ripple Current
CMS			118	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			29	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.29	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.86	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.29	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			-	Volts	Peak Drain Voltage is highly dependent on Transformer capacitance and leakage inductance. Please verify this on the bench and ensure that it is below 650 V to allow 50 V margin for transformer variation.
PIVS			39	Volts	Output Rectifier Maximum Peak Inverse Voltage

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8 Transformer Specification

8.1 Electrical Diagram

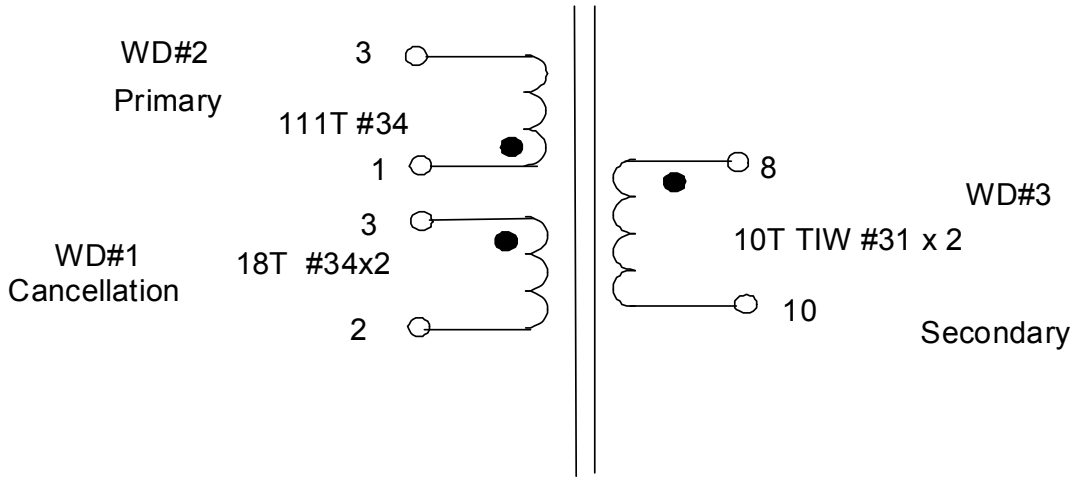


Figure 5 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-5 to pins 6-10	3000 VAC
Primary Inductance	Pins 3-1, all other windings open, measured at 100 kHz, 0.4 VRMS	2.287 mH, ±10%
Resonant Frequency	Pins 3-1, all other windings open	300 kHz (Min.)
Primary Leakage Inductance	Pins 1-3, with pins 10-8 shorted, measured at 100 kHz, 0.4 VRMS	50 μH (Max.)

8.3 Materials

Item	Description
[1]	Core: PC44 EE16, TDK or equivalent Gapped for ALG of 186 nH/T^2
[2]	Bobbin: Horizontal 10 pin
[3]	Magnet Wire: #34 AWG
[4]	Triple Insulated Wire: #31 AWG
[5]	Tape: 3M 1298 Polyester Film, 2.0 mils thick, 9.8 mm wide

8.4 Transformer Build Diagram

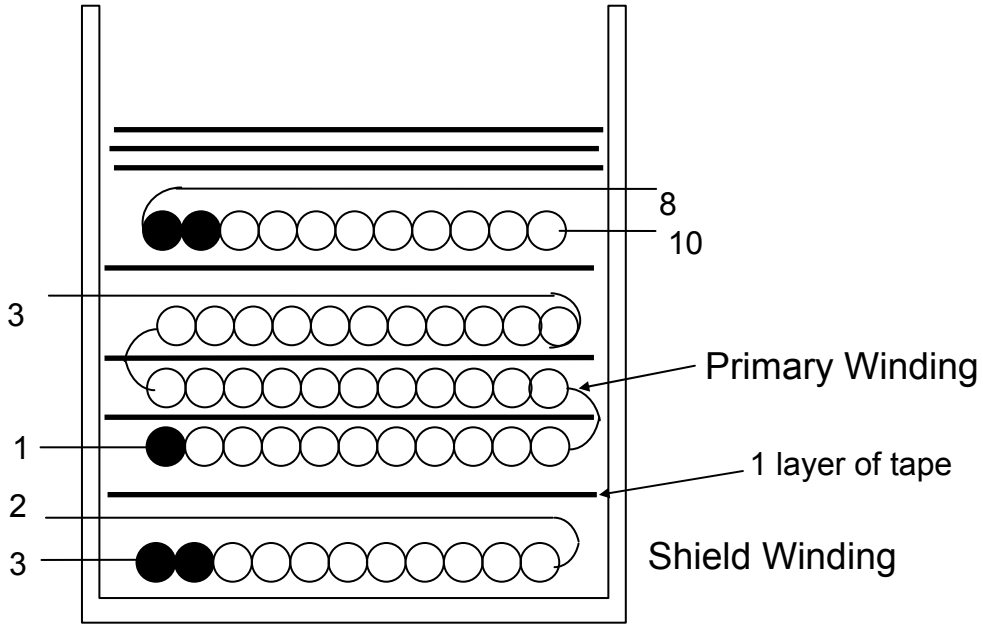


Figure 6 – Transformer Build Diagram.

8.5 Transformer Construction

Bobbin Preparation	Orient the bobbin such that the primary side pins of the bobbin are to the left hand side.
WD #1 Feedback	Start on pin 3, wind 18 bifilar turns of item [3] from left to right. Wind with tight tension across entire bobbin evenly. Finish on pin 2.
Insulation	1 Layers of tape [5] for insulation
WD #2 Primary	Start on pin 1, wind 37 turns of item [3] from left to right. After finishing the first layer, placing one layer of tape [5]. Continue to wind the second layer the wire from right to left with another 37 turns. After finishing the second layer, placing one layer of tape [5]. Continue to wind the wire from left to right with another 37 turns. Finish on pin 3.
Insulation	1 layer of tape [5] for insulation.
WD #3 Secondary	Start at pin 8, wind 10 bifilar turns of item [4] from left to right. Wind uniformly. After finishing the 10^{th} turn, bring the wire back and finish it on pin 10.
Insulation	3 layers of tape [5] for insulation.
Grind core	Grind the core to get 2.265 mH. Secure the core with tape. Vanish.
Finish	Secure the core with tape. Vanish.

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9 Performance Data

All measurements performed at room temperature and 50 Hz input frequency, except where otherwise stated. For all tests, the full load is 300 mA.

9.1 Active Mode Efficiency

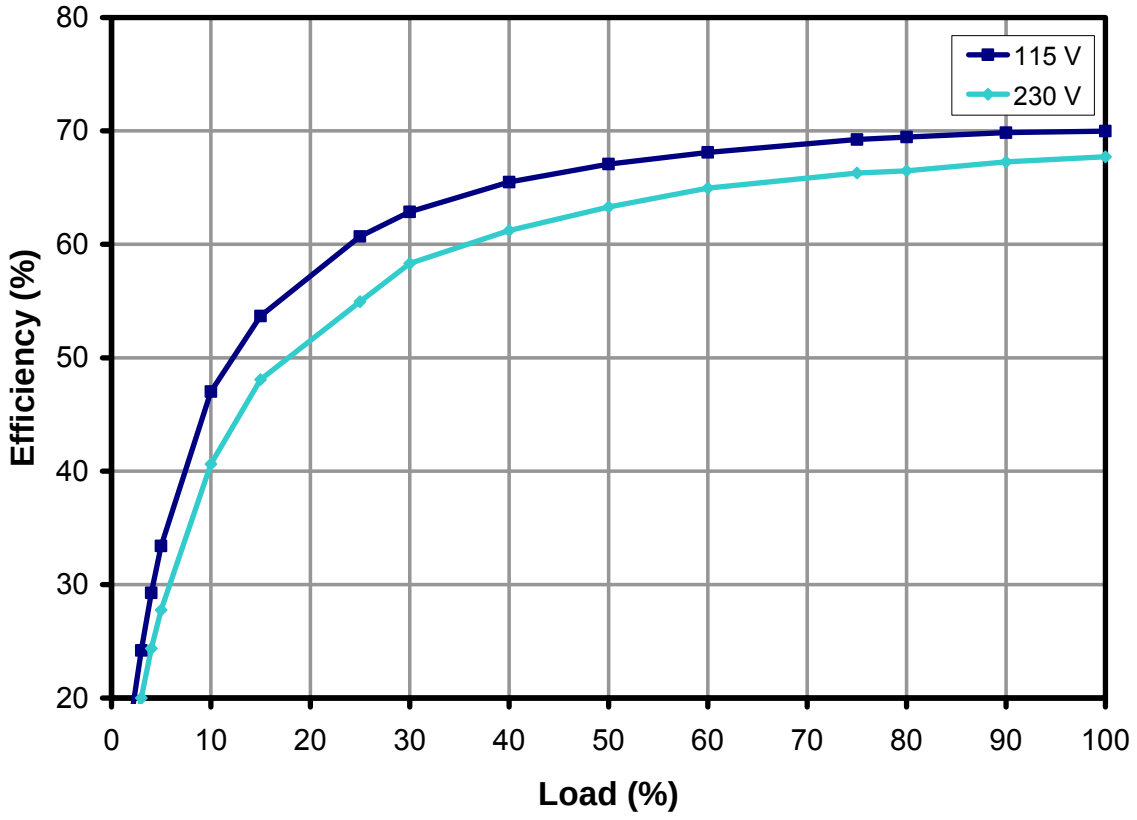


Figure 7- Efficiency vs. Input Voltage, Room Temperature, 50 Hz.

Percent of Full Load	Efficiency (%)	
	115 VAC	230 VAC
25	60.7	55.0
50	67.1	63.3
75	69.5	66.3
100	70.0	67.7
Average	66.8	63.1

9.2 No-load Input Power (Not in Power Down Mode)

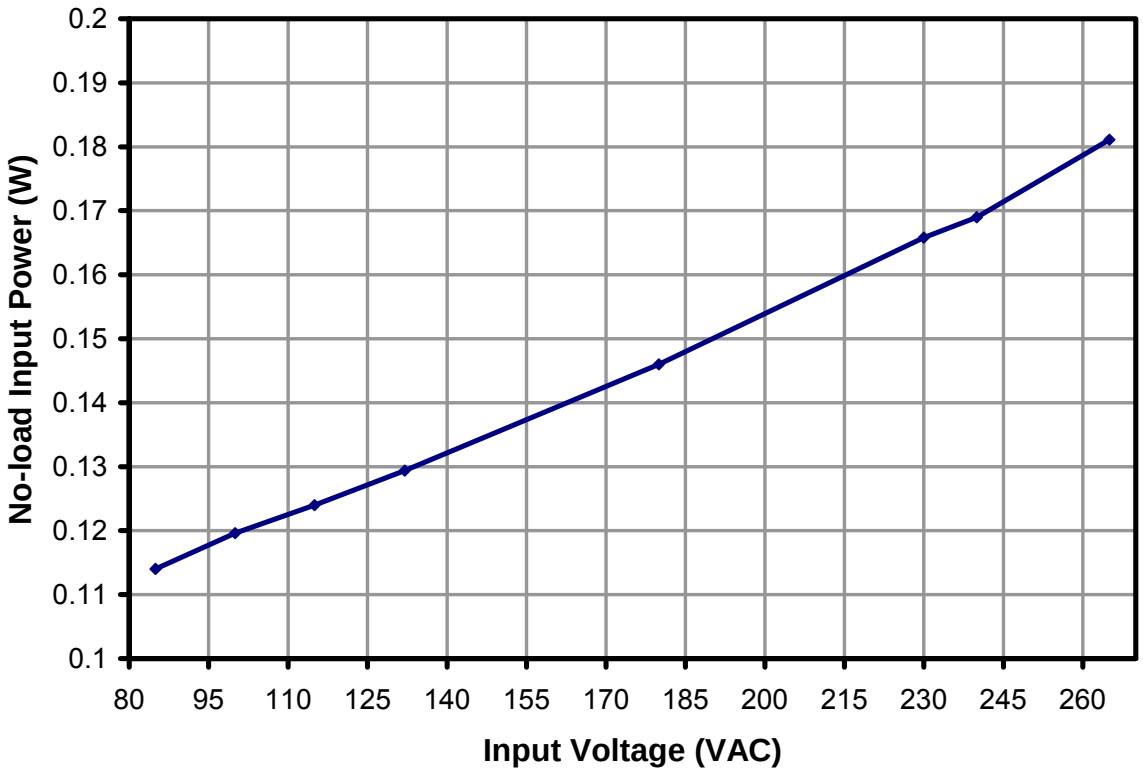


Figure 8 – No-load Input Power vs. Input Line Voltage, 25ºC, 50 Hz.

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9.3 No-load Input Power in Power Down Mode

The chart below shows the no load input power when in power down mode. In this mode, the input power is typically less than 5 mW at 230 VAC. The input power must be tested after 30 minutes to allow for the leakage currents of the bulk capacitors to stabilize. Power readings taken before this period will be higher. Also all measurements must be made without any multi meter or probes attached to the board as these tend to load the input.

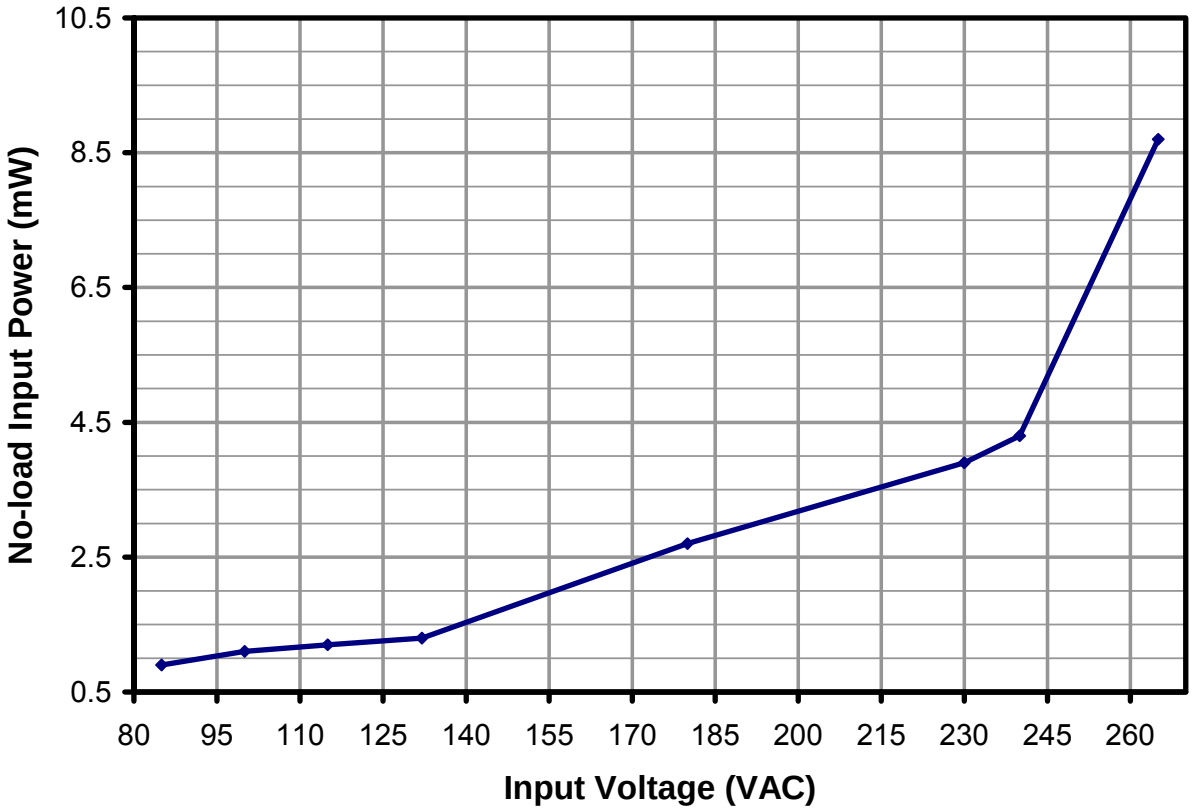


Figure 9 – No-load Input Power in PD mode vs. Input Line Voltage, 25 ºC, 50 Hz. 30 Minute Dwell Time at 230 VAC Prior to Taking Measurements.

9.4 Available Standby Output Power

The chart below shows the available output power vs. line voltage for an input power of 0.5 W and 1.0 W.

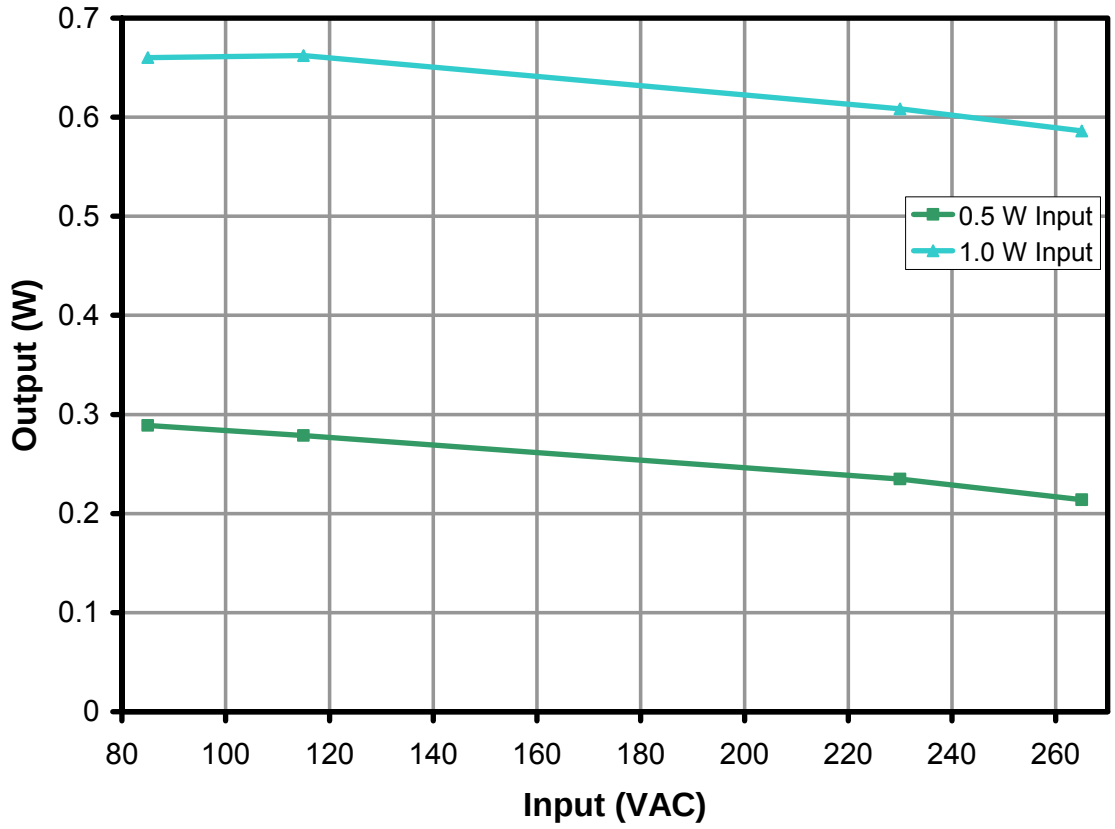


Figure 10 – Available Output Power for 0.5 W and 1 W Input Power.

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9.5 Line Regulation

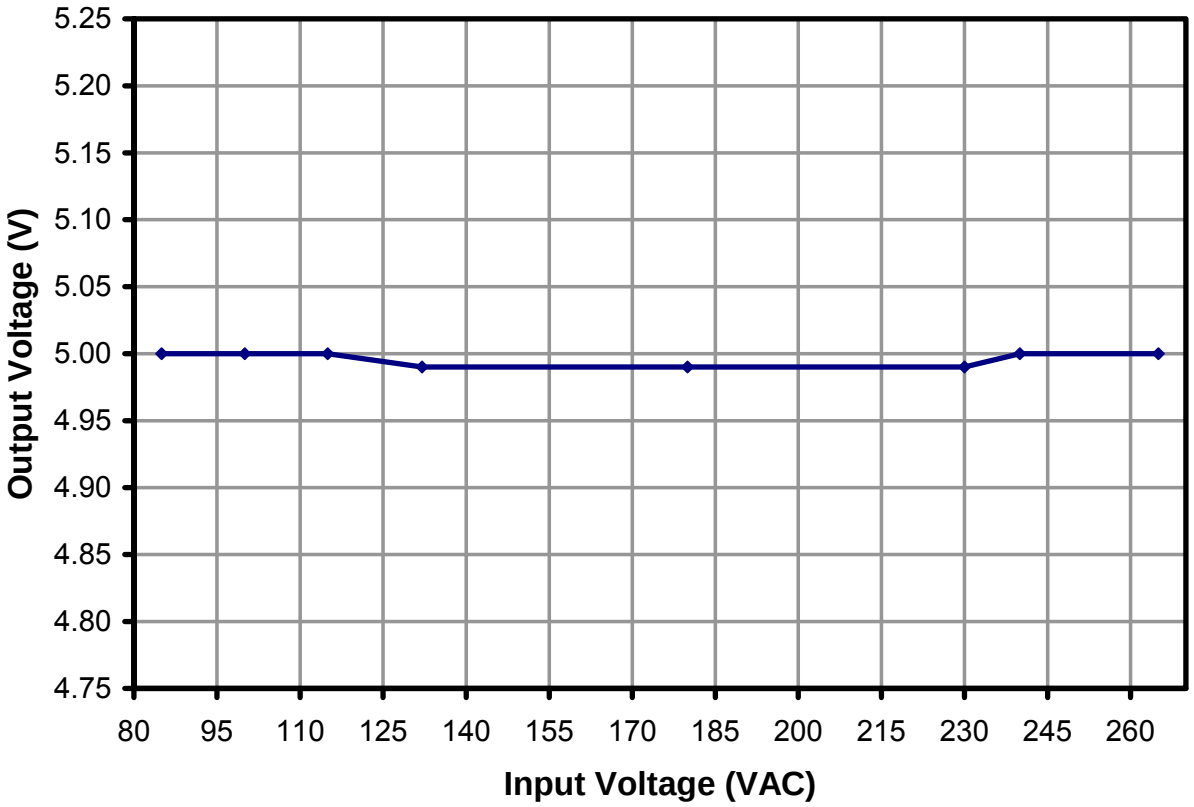


Figure 11 – Full Load Regulation at Room Ambient.

9.6 Load Regulation

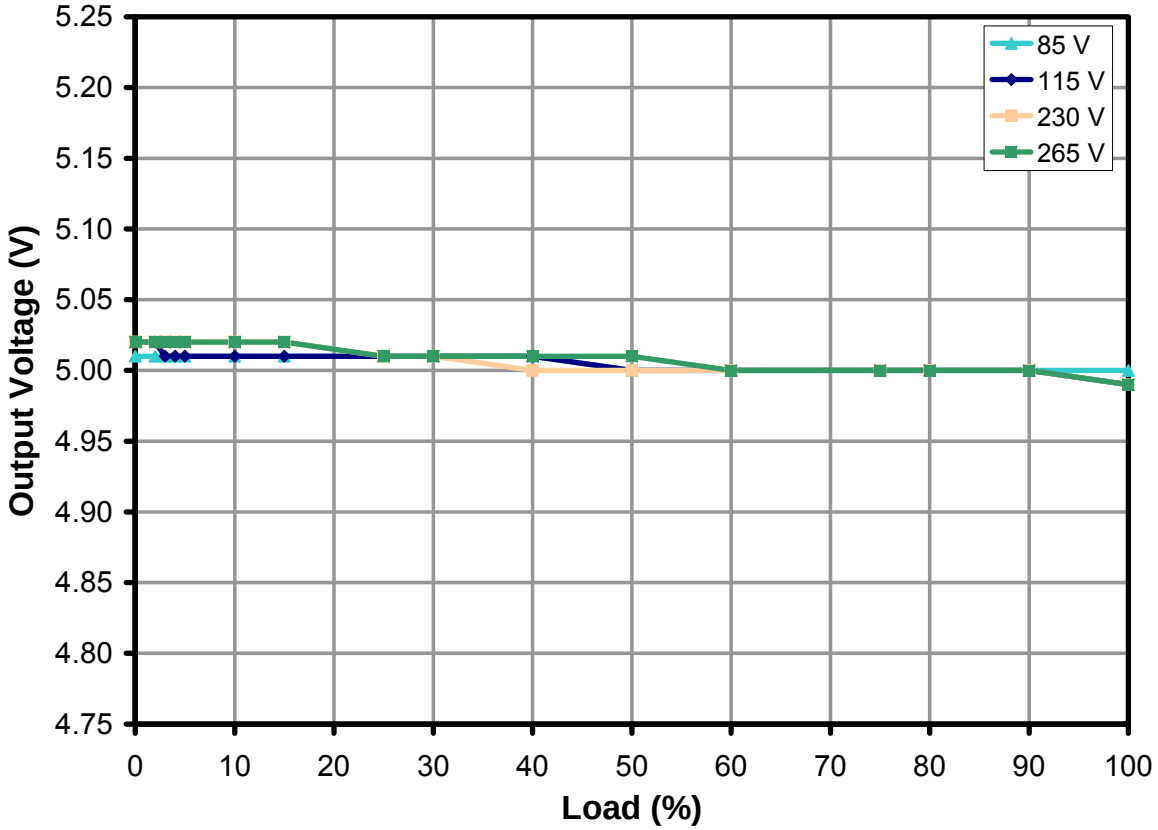


Figure 12 – Load Regulation at Room Ambient.

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10 Thermal Performance

Temperature measurements of key components were taken using T-type (Copper-Constantan) thermocouples. The thermocouples were soldered directly to a Source pin of the LNK584DG device and to the cathode of the output rectifier. The thermocouples were glued to the external core and to winding surfaces of the transformer.

The unit was sealed inside a large box to eliminate any air currents. The box was placed inside a thermal chamber. The ambient temperature within the large box was raised to 50 °C. The unit was then operated at full load and the temperature measurements were taken after they stabilized for 1 hour at 50 °C.

Temperature (°C)		
Item	**85 VAC**	**265 VAC**
Ambient inside the box	51.0	51.0
LN584DG (U1)	64	68
Output diode	71	73
Transformer	60	61

These results show that the IC has an acceptable rise in temperature.

11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

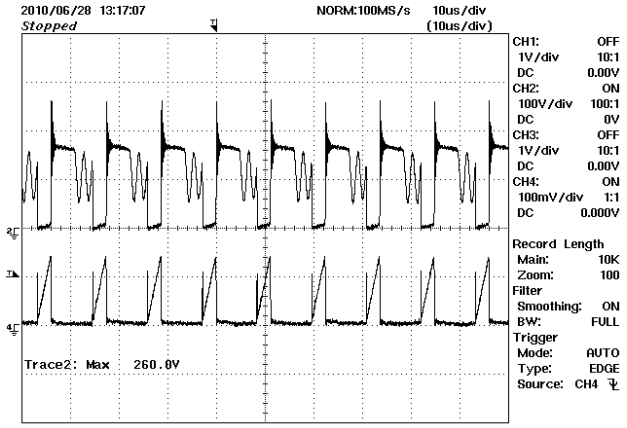


Figure 13 – 85 VAC, Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.1 A, 10 µs / div.

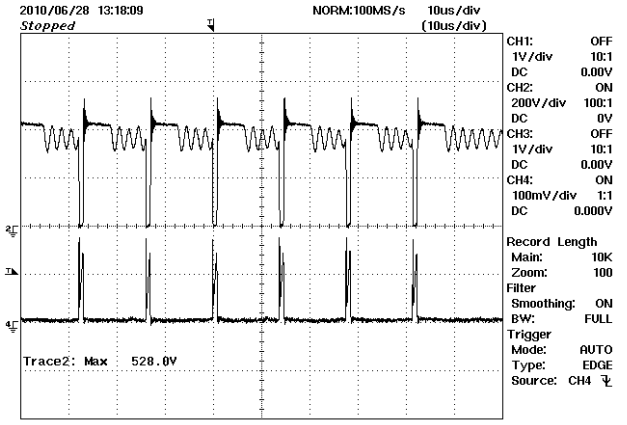


Figure 14 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.1 A, 10 µs / div.

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11.2 Output Voltage Start-up Profile with Input Voltage

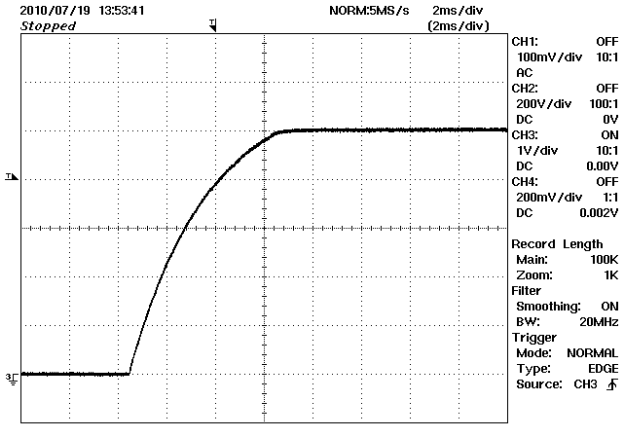


Figure 15 – Start-up Profile, 85 VAC, Full load, 1 V / div., 2 ms / div.

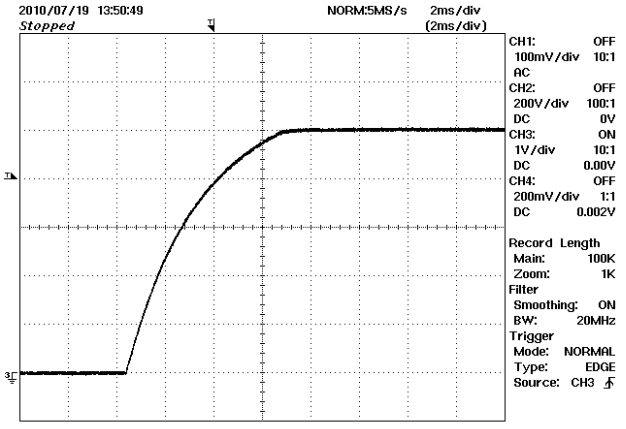


Figure 16 – Start-up Profile, 115 VAC, Full load, 1 V / div., 2 ms / div.

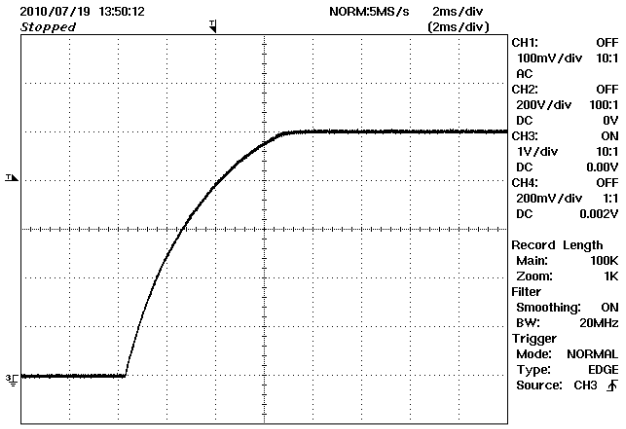


Figure 17 – Start-up Profile, 230 VAC, Full load, 1 V / div., 2 ms / div.

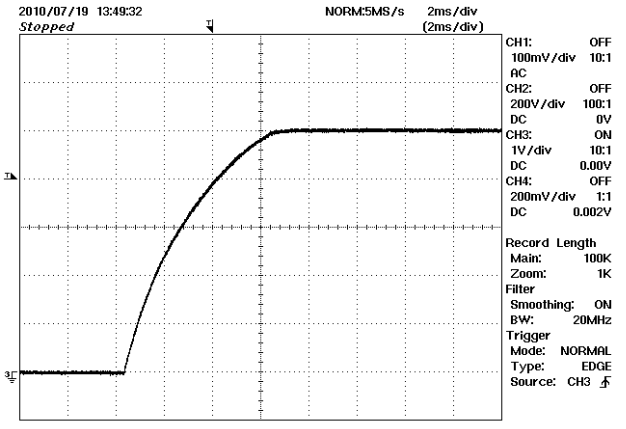


Figure 18 – Start-up Profile, 265 VAC, Full load, 1 V / div., 2 ms / div.

11.3 Power Down Mode Reset via Q2

When U1 is reset from the power down mode, notice how the output starts increasing after the BP pin voltage reaches 5.8 V.

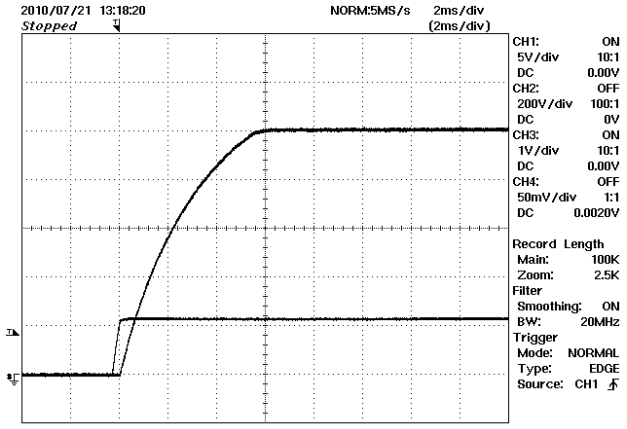


Figure 19 – Start-up Profile, 85 VAC, Full Load,
Upper: V_O, 1 V / div., 2 ms / div.
Lower: V_{BP}, 5 V / div.

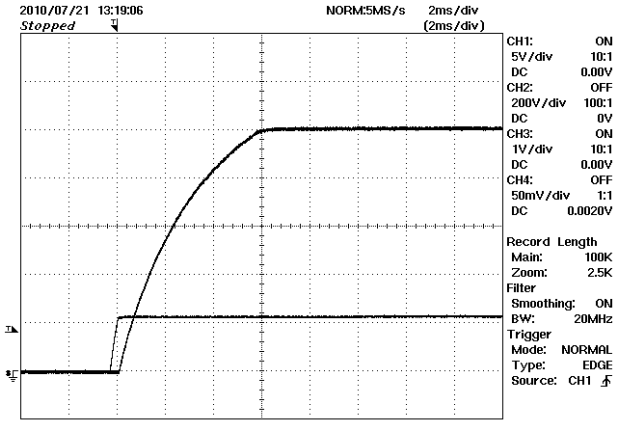


Figure 20 – Start-up Profile, 115 VAC, Full Load,
Upper: V_O, 1 V / div., 2 ms / div.
Lower: V_{BP}, 5 V/ div.

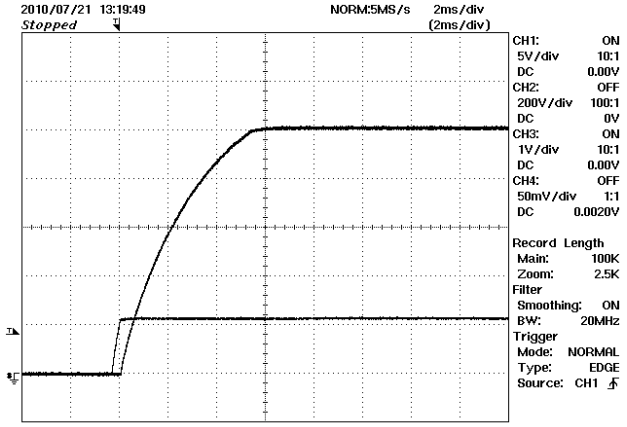


Figure 21 – Start-up Profile, 230 VAC, Full Load,
Upper: V_O, 1 V / div., 2 ms / div.
Lower: V_{BP}, 5 V / div.

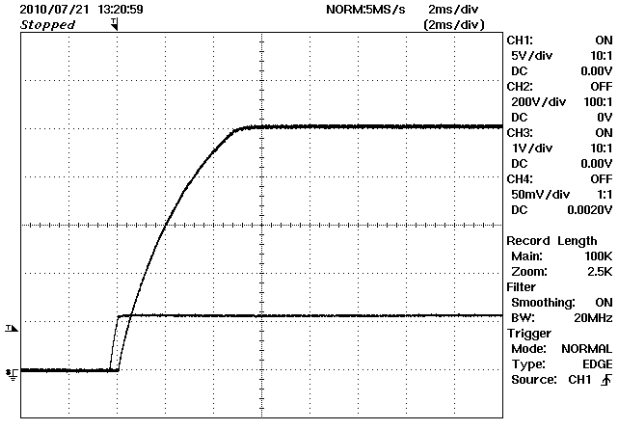


Figure 22 – Start-up Profile, 265 VAC, Full Load,
Upper: V_O, 1 V / div., 2 ms / div.
Lower: V_{BP}, 5 V / div.

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11.4 Power Down Mode Set via Switch Q1

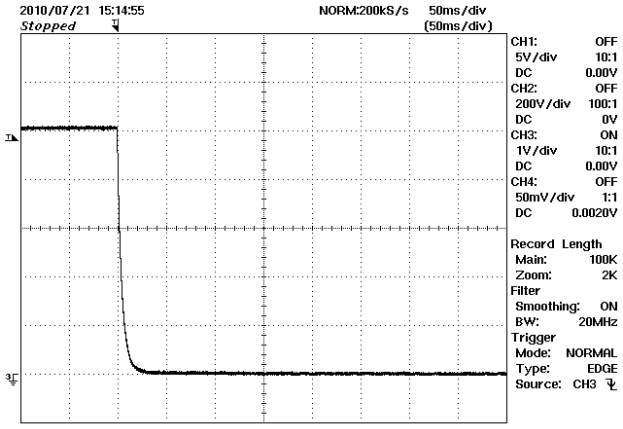


Figure 23 – Power Down Latch Off, 85 VAC, Full Load, 1 V / div., 50 ms / div.

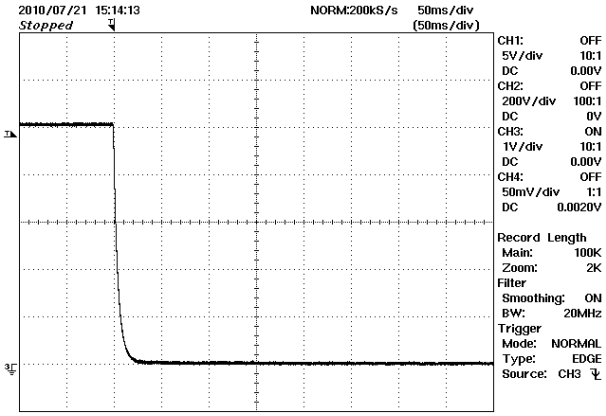


Figure 24 – Power Down Latch Off, 115 VAC, Full Load, 1 V / div., 50 ms / div.

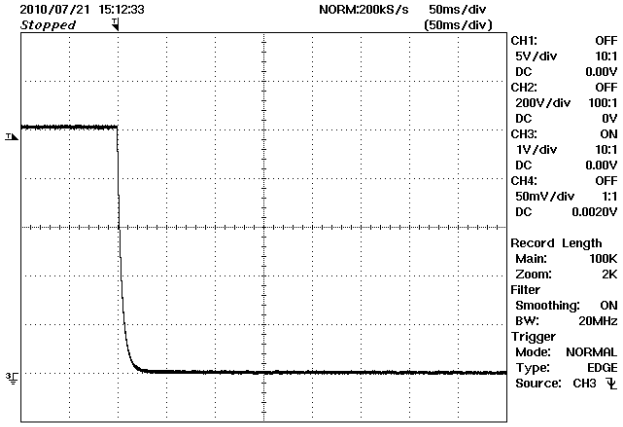


Figure 25 – Power Down Latch Off, 230 VAC, Full Load, 1 V / div., 50 ms / div.

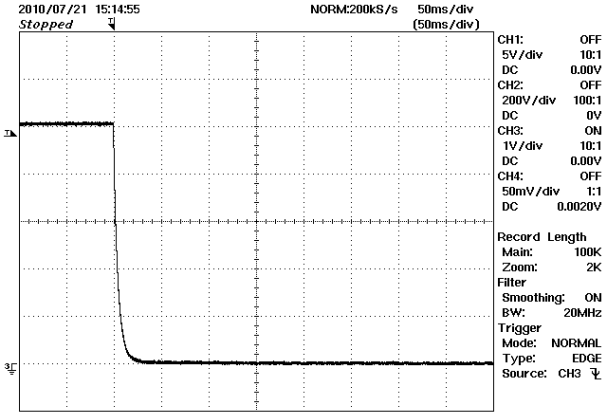


Figure 26 – Power Down Latch Off, 265 VAC, Full Load, 1 V / div., 50 ms / div.

11.5 Drain Voltage and Current Start-up Profile

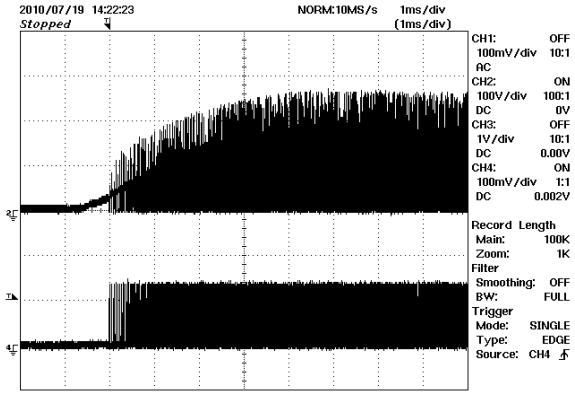


Figure 27 – 85 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.1 A, 1 ms / div.

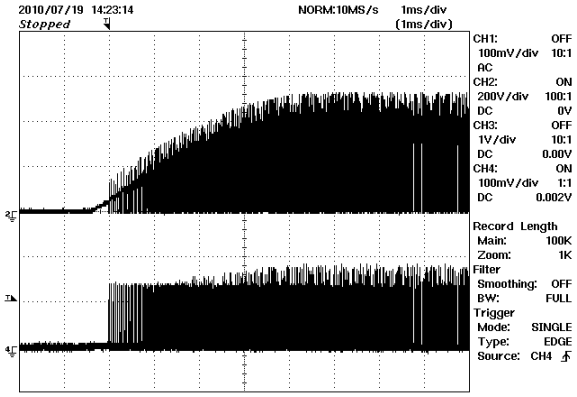


Figure 28 – 265 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.1 A, 1 ms / div.

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11.6 Load Transient Response

11.6.1 ~ 0% to 100% Load Step

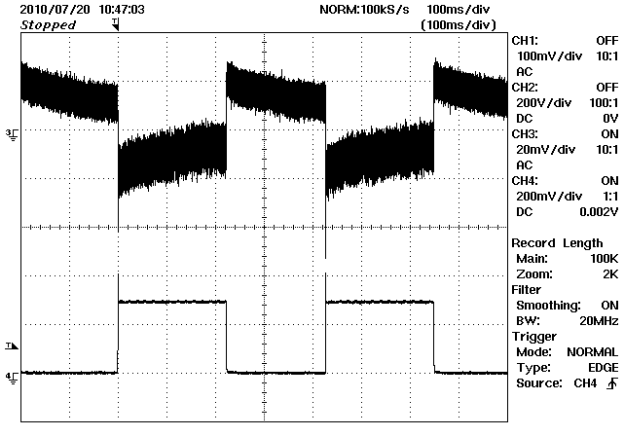


Figure 29 – Transient Response, 85 VAC,
4 mA – 300 mA – 4 mA,
Upper: V_O, 20 mV / div., 100 ms / div.
Lower: I_O, 0.2 A / div.

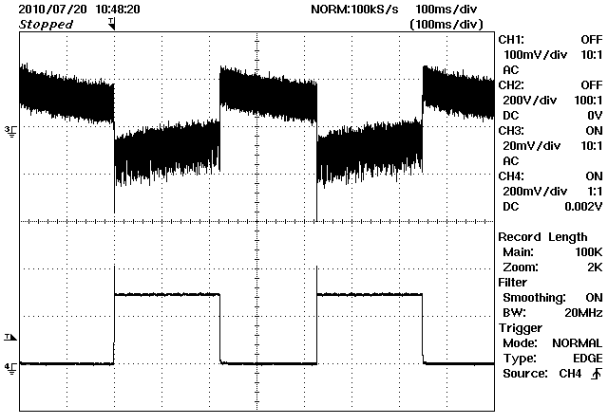


Figure 30 – Transient Response, 115 VAC
4 mA – 300 mA – 4 mA,
Upper: V_O, 20 mV / div., 100 ms / div.
Lower: I_O, 0.2 A / div.

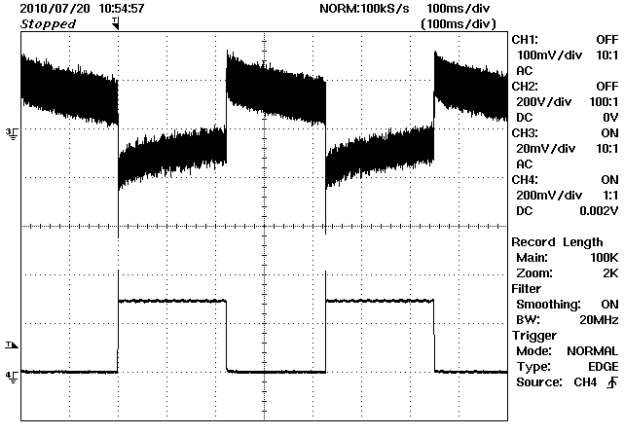


Figure 31 – Transient Response, 230 VAC,
4 mA – 300 mA – 4 mA,
Upper: V_O, 20 mV / div., 100 ms / div.
Lower: I_O, 0.2 A / div.

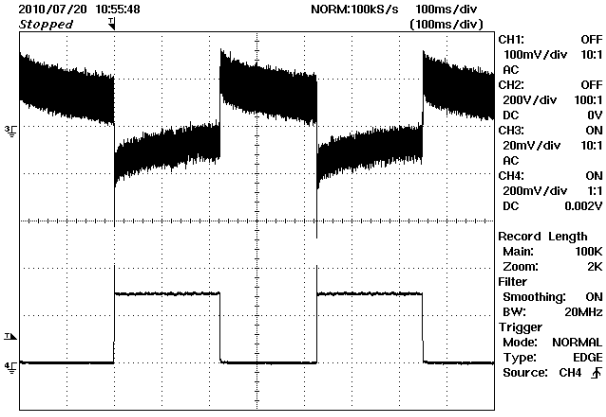


Figure 32 – Transient Response, 265 VAC,
4 mA – 300 mA – 4 mA,
Upper: V_O, 20 mV / div., 100 ms / div.
Lower: I_O, 0.2 A / div.

11.6.2 50% to 100% Load Step

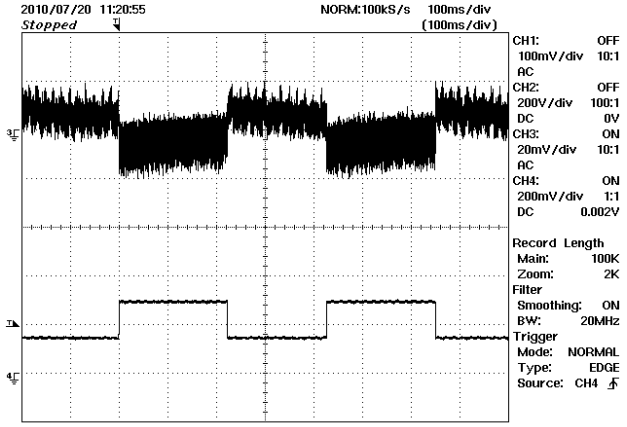


Figure 33 – Transient Response, 85 VAC,
150 mA – 300 mA – 150 mA,
Upper: V_O, 20 mV / div., 100 ms / div.
Lower: I_O, 0.2 A / div.

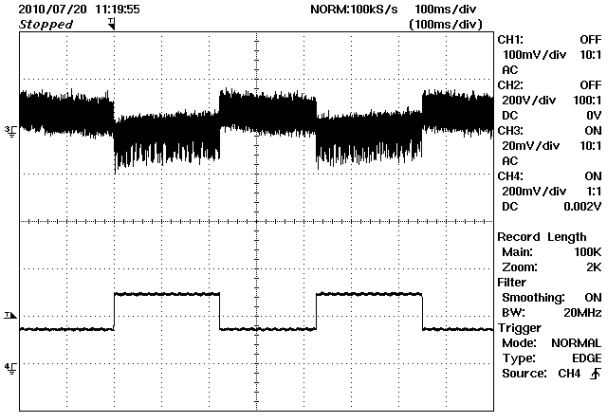


Figure 34 – Transient Response, 115 VAC,
150 mA – 300 mA – 150 mA,
Upper: V_O, 20 mV / div., 100 ms / div.
Lower: I_O, 0.2 A / div.

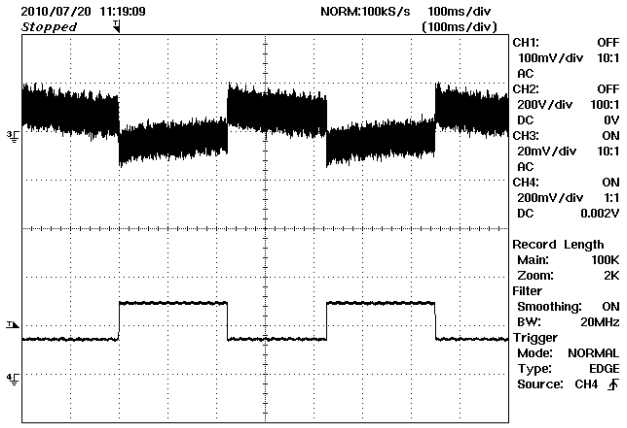


Figure 35 – Transient Response, 230 VAC,
150 mA – 300 mA – 150 mA,
Upper: V_O, 20 mV / div., 100 ms / div.
Lower: I_O, 0.2 A / div.

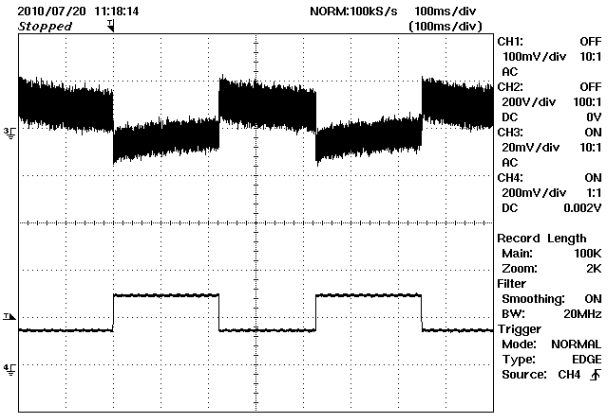


Figure 36 – Transient Response, 265 VAC,
150 mA – 300 mA – 150 mA,
Upper: V_O, 20 mV / div., 100 ms / div.
Lower: I_O, 0.2 A / div.

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11.6.3 100% to 0% (No-Load) Load Step

This following transient load tests verify that under extreme conditions of transient loads, power down mode is not triggered.

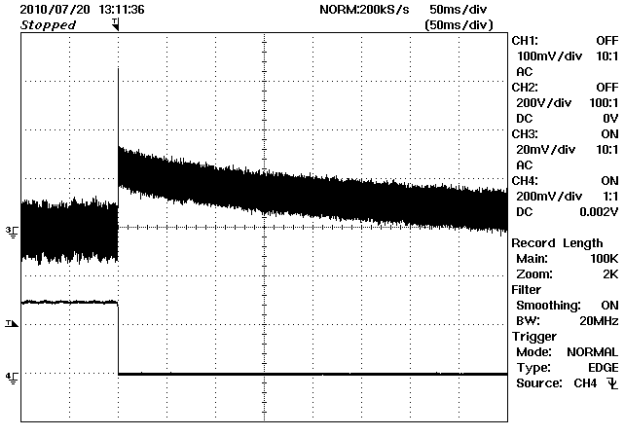


Figure 37 – Transient Response, 85 VAC, 300 mA – 0 mA
Upper: V_O, 20 mV / div., 50 ms / div.
Lower: I_O, 0.2 A /div.

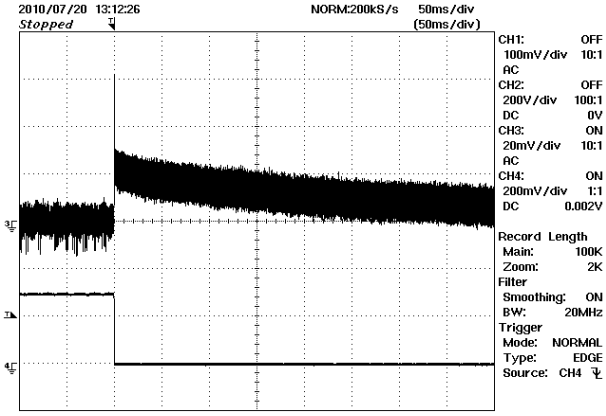


Figure 38 – Transient Response, 115 VAC, 300 mA – 0 mA
Upper: V_O, 20 mV / div., 50 ms / div.
Lower: I_O, 0.2 A / div.

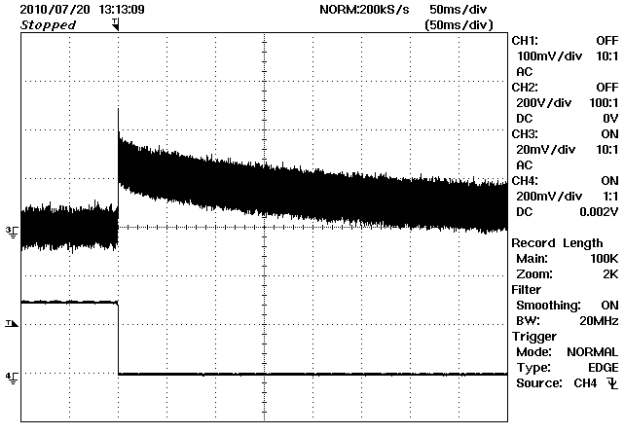


Figure 39 – Transient Response, 230 VAC, 300 mA – 0 mA
Upper: V_O, 20 mV / div., 50 ms / div.
Lower: I_O, 0.2 A / div.

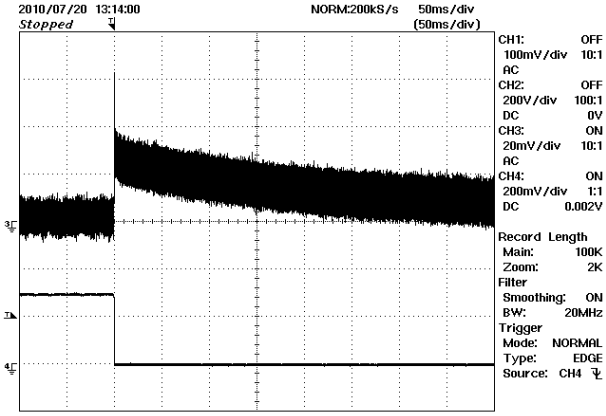


Figure 40 – Transient Response, 265 VAC, 300 mA – 0 mA
Upper: V_O, 20 mV / div., 50 ms / div.
Lower: I_O, 0.2 A / div.

11.6.4 0% to 100% Load Step

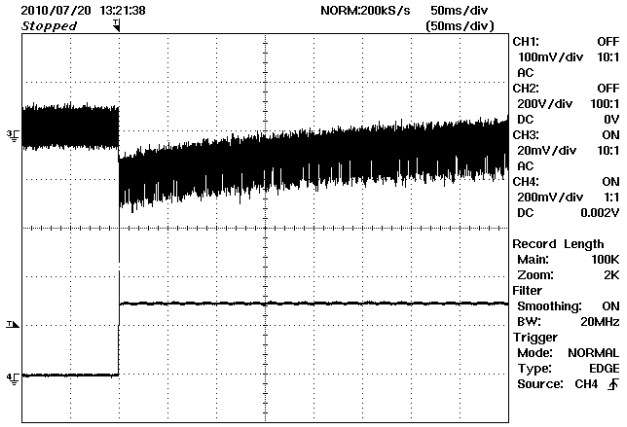


Figure 41 – Transient Response, 85 VAC,
0 mA – 300 mA
Upper: V_O, 20 mV / div., 50 ms / div.
Lower: I_O, 0.2 A / div.

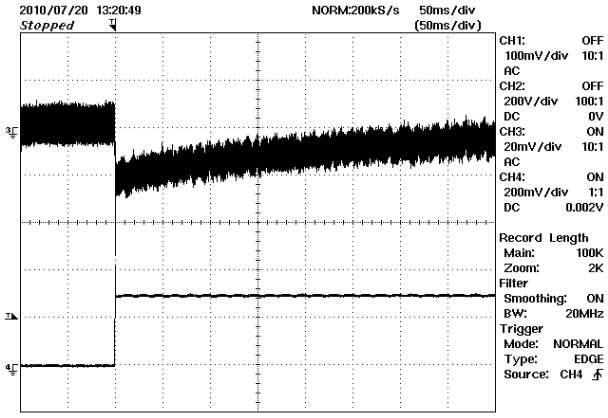


Figure 42 – Transient Response, 115 VAC,
0 mA – 300 mA
Upper: V_O, 20 mV / div., 50 ms / div.
Lower: I_O, 0.2 A / div.

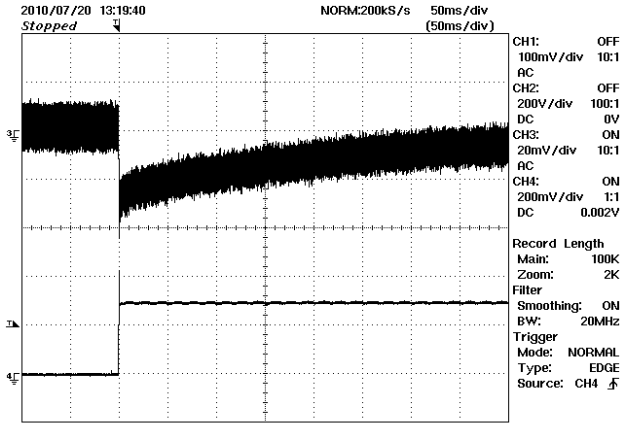


Figure 43 – Transient Response, 230 VAC,
0 mA – 300 mA
Upper: V_O, 20 mV / div., 50 ms / div.
Lower: I_O, 0.2 A / div.

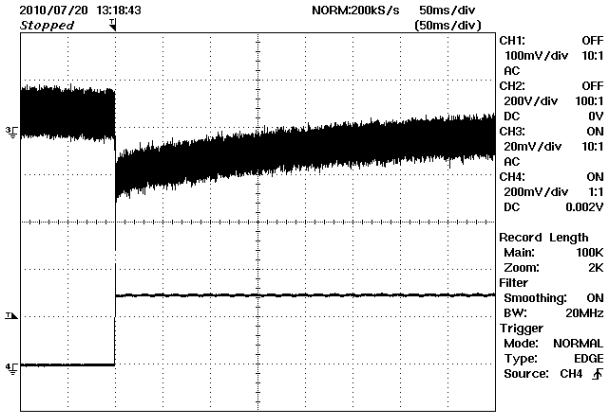


Figure 44 – Transient Response, 265 VAC,
0 mA – 300 mA
Upper: V_O, 20 mV / div., 50 ms / div.
Lower: I_O, 0.2 A / div.

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11.7 Output Ripple Measurements

11.7.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in the figures below.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

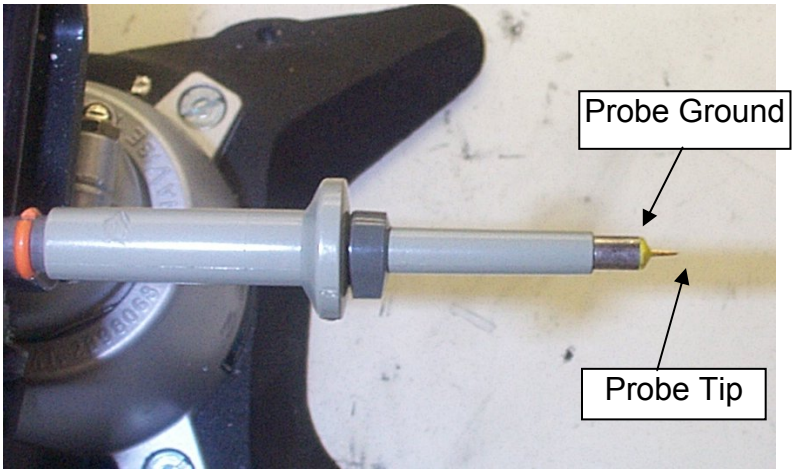


Figure 45 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

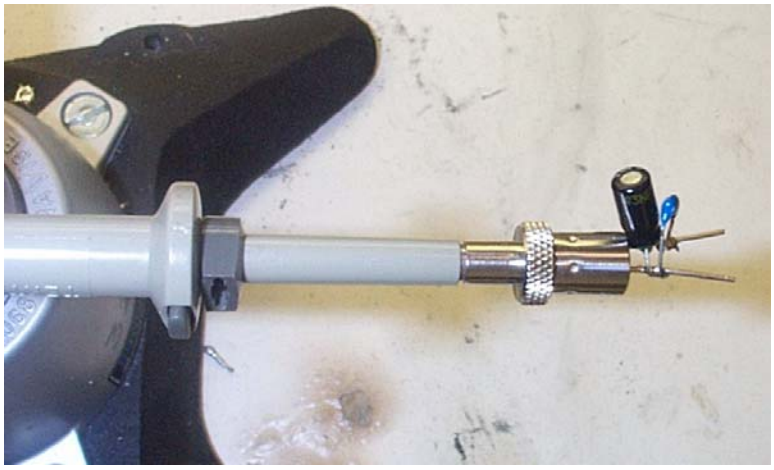


Figure 46 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)

11.7.2 Measurement Results at 25˚C Ambient Temperature

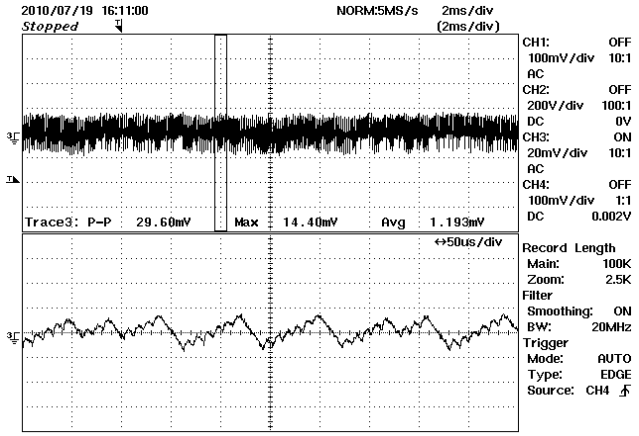


Figure 47 – Output Ripple, 85 VAC, Full Load,
Upper: Ripple, 2 ms, 20 mV / div.
Lower: Ripple, 50 μs, 20 mV / div.

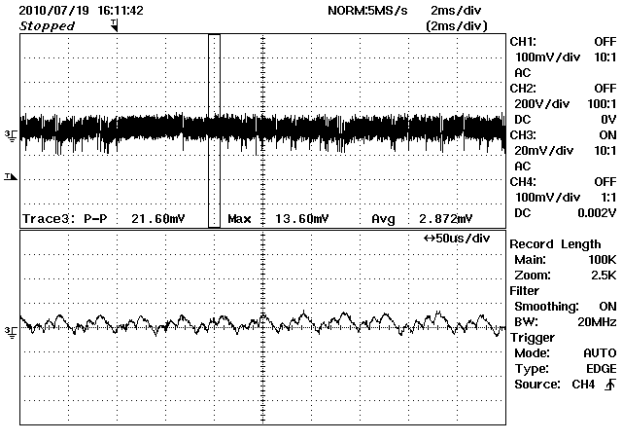


Figure 48 – Output Ripple, 115 VAC, Full Load,
Upper: Ripple, 2 ms, 20 mV / div.
Lower: Ripple, 50 μs, 20 mV / div.

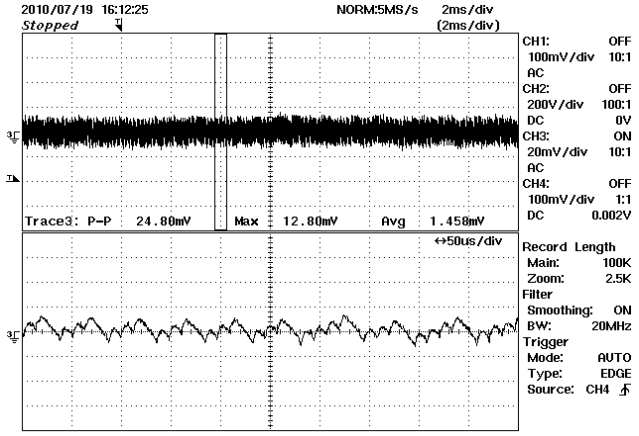


Figure 49 – Output Ripple, 230 VAC, Full Load,
Upper: Ripple, 2 ms, 20 mV / div.
Lower: Ripple, 50 μs, 20 mV / div.

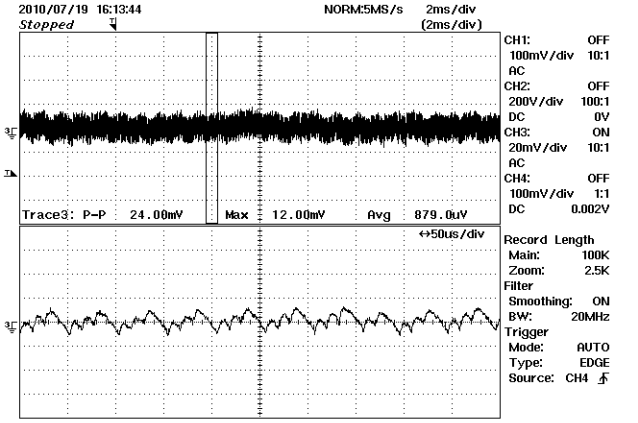


Figure 50 – Output Ripple, 265 VAC, Full Load,
Upper: Ripple, 2 ms, 20 mV / div.
Lower: Ripple, 50 μs, 20 mV / div.

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11.8 Output Short-Circuit at Room Ambient

In the event of a short circuit on the output, the LNK584DG enters auto-restart mode. In this protection model, switching is disabled. The auto-restart alternately enables and disables the switching of the power MOSFET at a duty cycle of typically 12% until the fault condition is removed.

11.8.1 Auto-Restart On/Off Time Test

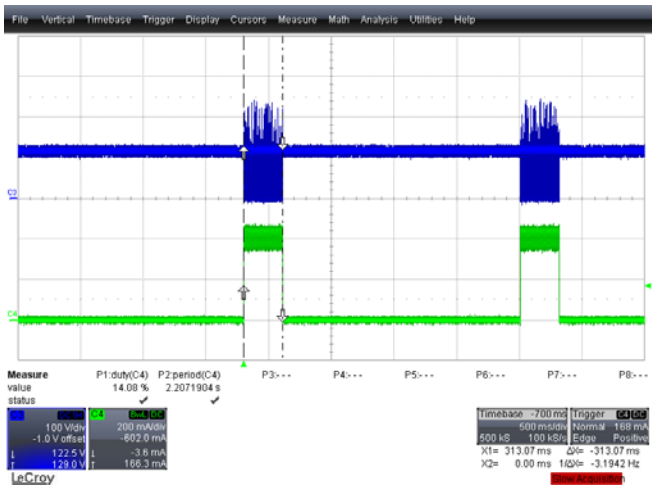


Figure 51 – 85 VAC Input, Short-Circuit.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.2 A, 500 ms / div.
Auto-restart On Time, 313 ms. Auto-restart Off Time, 1.9 s**.**

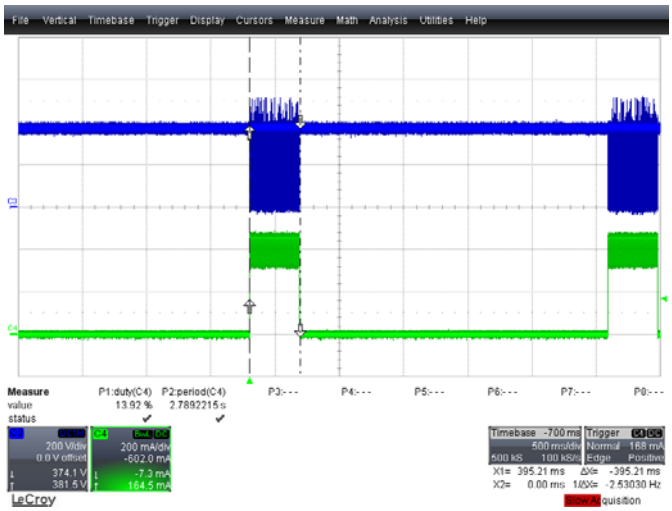


Figure 52 – 265 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A, 20 µs / div.
Auto-restart On Time, 395 ms. Auto-restart Off Time, 2.4 s

11.8.2 Drain Voltage and Current Under Output Short-Circuit

The waveforms show that there is no saturation of the transformer under output short circuit and the voltage stress is also below the 700 V BV_{DSS} rating of the LNK584DG.

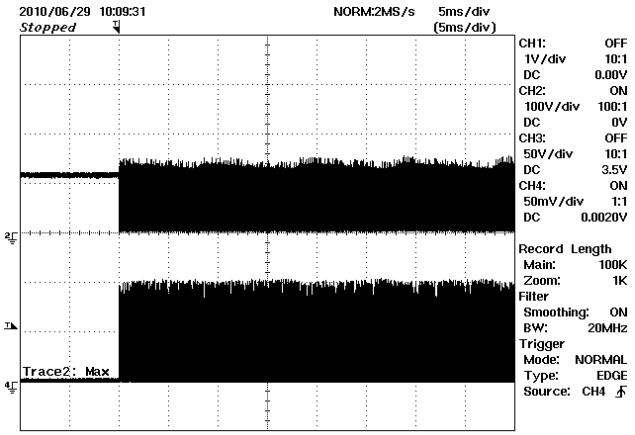


Figure 53 – 85 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.05 A, 5 ms / div.

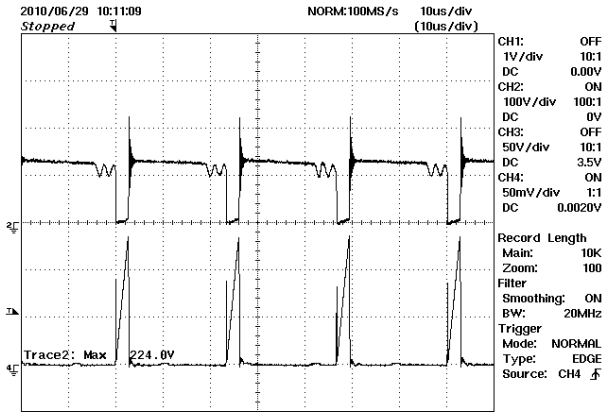


Figure 54 – 85 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.05 A, 20 μs / div.

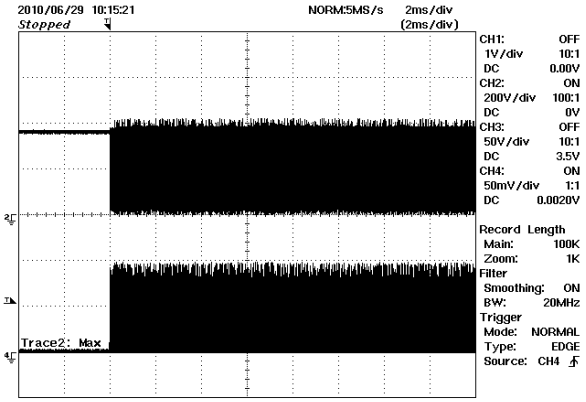


Figure 55 – 265 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.05 A, 5 ms / div.

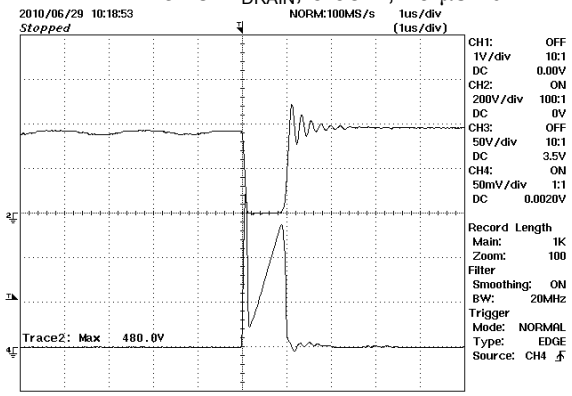


Figure 56 – 265 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.05 A, 1 μs / div.

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12 Line Surge

Input line 1.2/50 µs common-mode and differential mode surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event. Test conditions and results are shown below.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Line Impedance (Ω)	Injection Phase (°)	Number of Surges	Test Result (Pass/Fail)
+1000	230	L to N	2	90	10	Pass
-1000	230	L to N	2	270	10	Pass
+2000	230	L/N to GND	12	90	10	Pass
-2000	230	L/N to GND	12	270	10	Pass

Units passed under all test conditions.

13 EMI Tests at Full Load

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load. Composite EN55022B / CISPR22B conducted limits are shown. All the tests show excellent EMI performance.

13.1 EMI Results

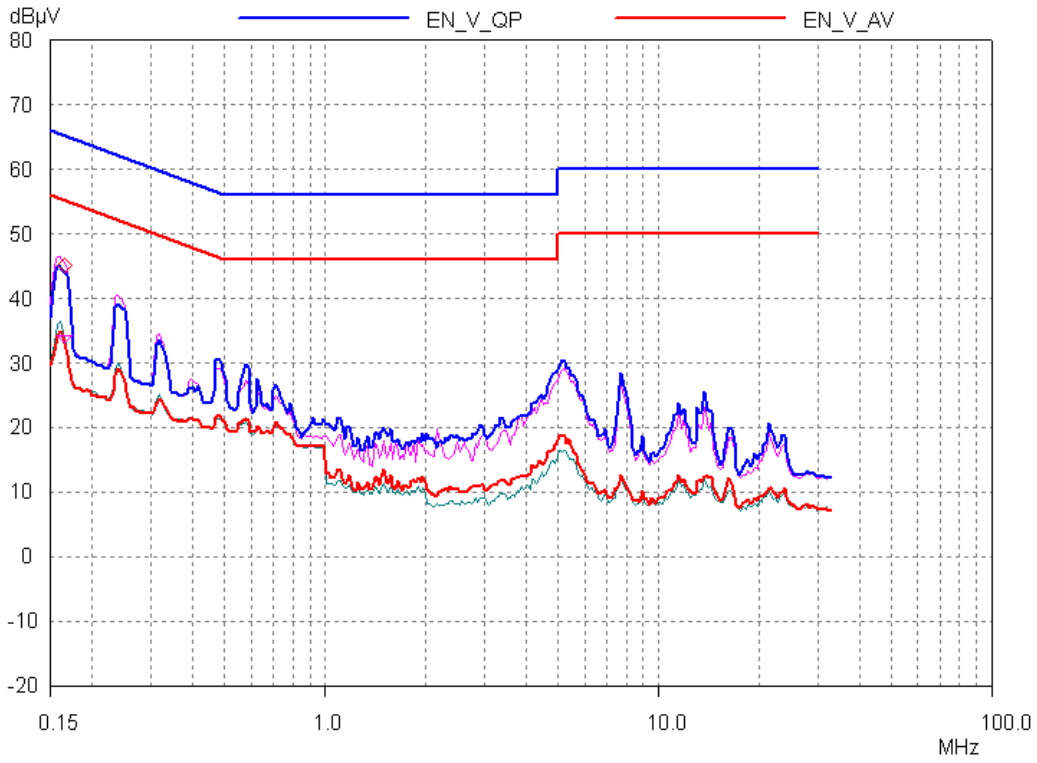


Figure 57 – Conducted EMI at 115 VAC 60 Hz, 0.3 A Load, Secondary Ground Connected to Artificial Hand.

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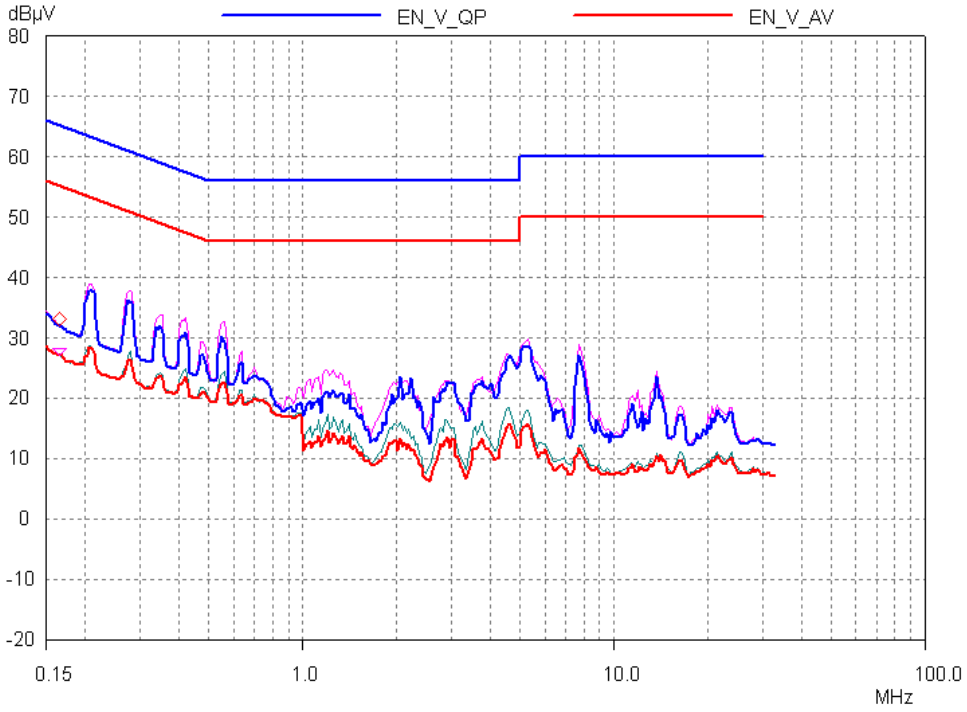


Figure 58 – Conducted EMI at 230 VAC 60 Hz, 0.3 A Load, Secondary Ground Connected to Artificial Hand.

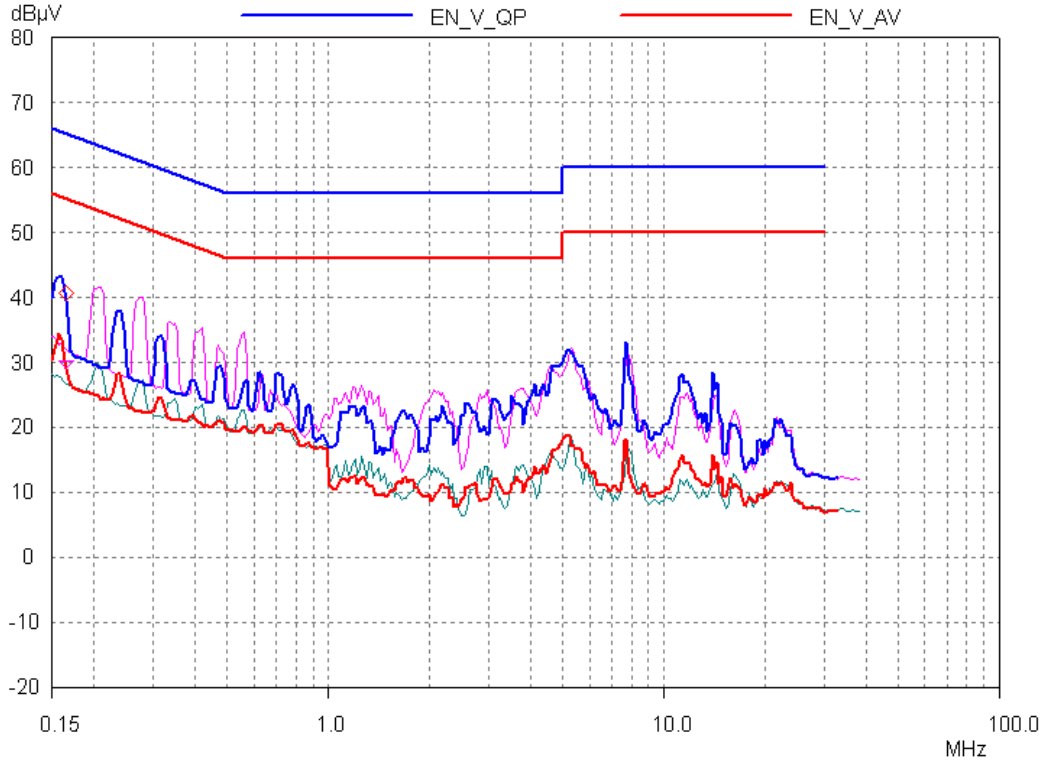


Figure 59 – Conducted EMI at 115 VAC 60 Hz, 0.3 A Load, Secondary Ground Floating.

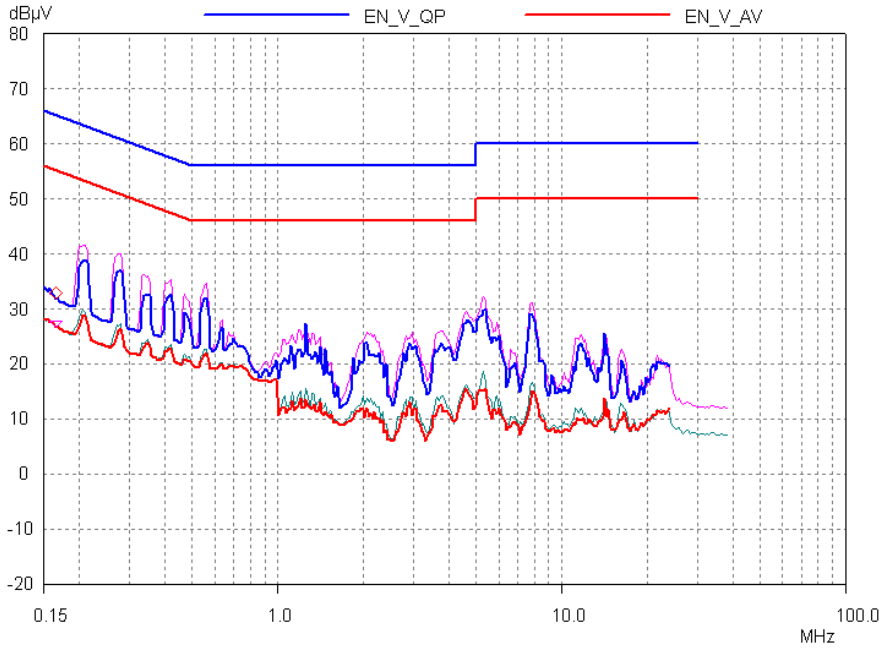


Figure 60 – Conducted EMI at 230 VAC 60 Hz, 0.3 A Load, Secondary Ground Floating

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Tel: +1 408 414 9200 Fax: +1 408 414 9201
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14 Revision History

Date	Author	Revision	Description & changes	Reviewed
13-Oct-10	PL	1.3	Initial Release	Apps & Mktg

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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail:
usasales@powerint.com

GERMANY
Rueckertstrasse 3
D-80336, Munich
Germany
Phone: +49-89-5527-3911
Fax: +49-89-5527-3920
e-mail:
eurosales@powerint.com

JAPAN
Kosei Dai-3 Building
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

TAIWAN
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu District
Taipei 114, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail:
taiwansales@powerint.com

CHINA (SHANGHAI)
Rm 1601/1610, Tower 1
Kerry Everbright City
No. 218 Tianmu Road West
Shanghai, P.R.C. 200070
Phone: +86-021-6354-6323
Fax: +86-021-6354-6325
e-mail:
chinasales@powerint.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail:
indiasales@powerint.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728
Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

UNITED KINGDOM
1st Floor, St. James's House
East Street,
Farnham Surrey, GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-141
Fax: +44 (0) 1252-727-689
e-mail:
eurosales@powerint.com

CHINA (SHENZHEN)
Rm A, B & C 4th Floor, Block C,
Electronics Science and
Technology Building
2070 Shennan Zhong Road
Shenzhen, Guangdong,
P.R.C. 518031
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail:
chinasales@powerint.com

ITALY
Via De Amicis 2
20091 Bresso MI
Italy
Phone: +39-028-928-6000
Fax: +39-028-928-6009
e-mail:
eurosales@powerint.com

SINGAPORE
51 Newton Road,
#15-08/10 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail:
singaporesales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760