Application Note AN-61
LinkSwitch-3 Family

Design Guide and Considerations

Introduction

LinkSwitch™-3 family of ICs are highly integrated monolithic switching ICs designed for off-line power supplies with output power up to 10 W. Ideally suited for chargers, adapters, auxiliary supplies and LED drivers, LinkSwitch-3 provides constant voltage and constant current (CV/CC) output regulation without using an optocoupler or secondary feedback circuitry. The integrated output cable voltage drop compensation, transformer inductance compensation, and external component temperature variation compensation allow high accuracy even at the end of the output cable. ON/OFF control optimizes efficiency across load and line, enabling designs to easily meet no-load and power supply efficiency requirements.

Each member of this family has a high-voltage power MOSFET and its controller integrated onto the same die. The internal start-up bias current is drawn from a high-voltage current source connected to the DRAIN pin, eliminating the need for external start-up components. The internal oscillator is frequency-modulated (jitter) to reduce EMI when operating in full frequency mode. In addition, the ICs have integrated functions that provide system-level protection. The auto-restart function limits dissipation in the MOSFET, the transformer, and the output diode during overload, output short-circuit, and open-loop conditions. The auto-recovering hysteretic thermal shutdown function disables MOSFET switching during a thermal fault. Power Integrations' EcoSmart™ technology enables power supplies designed around the LinkSwitch-3 family members to consume less than 30 mW of no-load power output with a low-cost bias circuit. This simplifies meeting harmonized energy efficiency standards such as the California Energy Commission (CEC), European Code of Conduct, and ENERGY STAR.

Basic Circuit Configuration

The circuit in Figure 1 shows the basic configuration of a flyback power supply designed using LinkSwitch-3. Because of the high-level integration of LinkSwitch-3, far fewer design issues are left to be addressed externally, resulting in one common circuit configuration for all applications. For example, different output power levels may require different values for some circuit components, but the circuit configuration stays unchanged.

Scope

This application note is intended for engineers designing an isolated AC-DC flyback power supply using the LinkSwitch-3 family of devices. It provides guidelines to enable an engineer to quickly select key components and to complete a suitable transformer design. To simplify the task this application note refers directly to the PIXls design spreadsheet, part of the PI Expert™ design software suite.

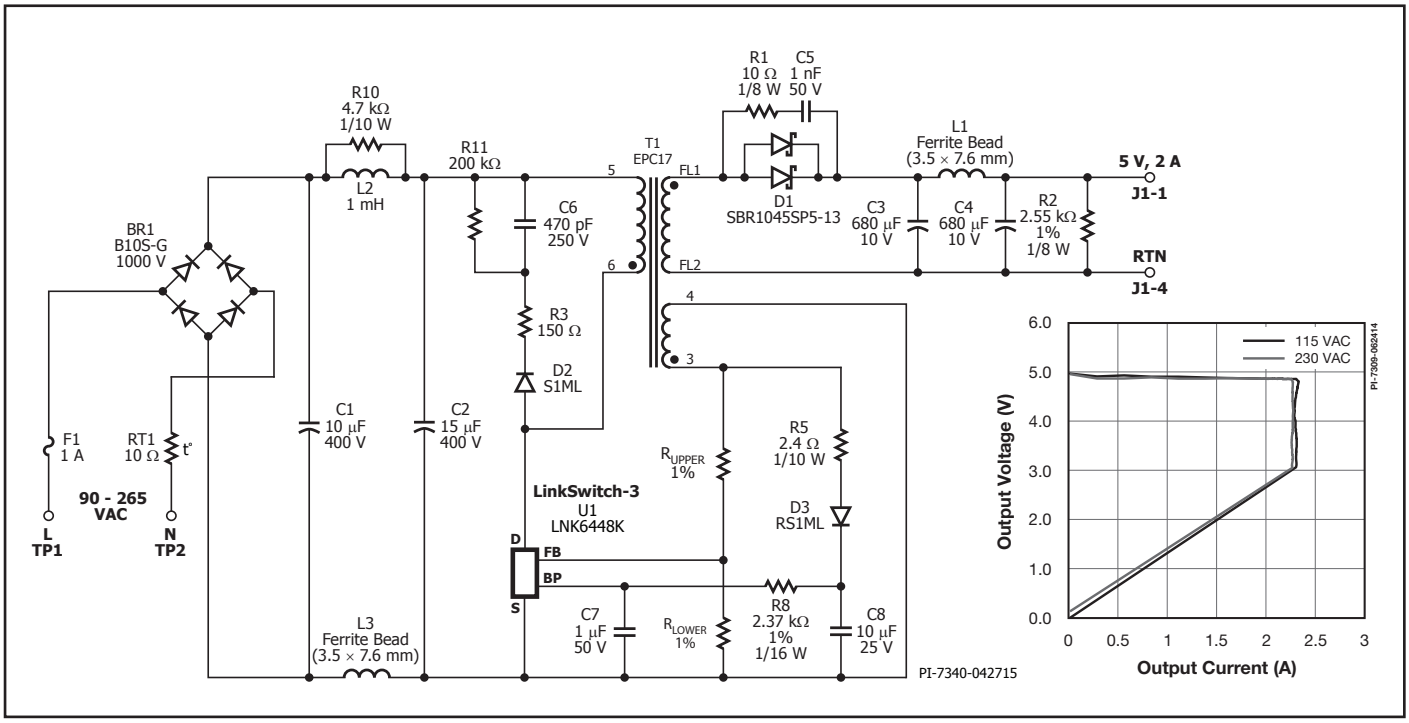

Figure 1. Energy Efficient USB Charger Power Supply (78% Average Efficiency, <30 mW No-load Input Power).

In addition to this application note, you may also find the LinkSwitch-3 Design Examples Reports (DER). Further details on downloading PI Expert, Design Example Reports, and updates to this document can be found at www.power.com.

Quick Start

To start immediately, use the following information to quickly design the transformer and select the components for a first prototype. Only the information described below needs to be entered into the PIXls spreadsheet; other parameters will be automatically selected based on a typical design. References to spreadsheet cell locations are provided in square brackets [cell reference].

- Enter AC input voltage range VAC_{MIN}, VAC_{MAX}, and minimum line frequency f_L [B3, B4, B5].
- Select the application type, either adapter or open frame [B6].
- Enter nominal output voltage (at end of cable if applicable) V_O [B7].
- Enter the minimum required output current value [B8].
- Enter efficiency estimate [B10].
  - 0.76 for universal input voltage (85-265 VAC) or single 100/115 VAC (85-132 VAC), 0.78 for a single 230 VAC (185-265 VAC) design. (Adjust the number as needed after measuring the efficiency of the first prototype-board at maximum load and VAC_{MIN}.)
- Enter loss allocation factor Z [B11].
  - 0.5 for typical application (adjust the number accordingly after first proto-board evaluation)
- Enter C_{IN} input capacitance [B13].
  - ≥2.5 μF/W for universal (85-265 VAC) or single (100/115 VAC) line voltage.
  - 1 μF/W for single 230 VAC or single (195-265 VAC) line voltage.
  - Note: After selecting the LinkSwitch-3 device, if the computed duty cycle [D64] is greater than 55%, increase the input capacitance.
- Select the LinkSwitch-3 device from the drop-down list.
  - Select the device in Table 1 according to output power.
- Select the cable drop compensation option from the drop-down list. The complete part number will be showed in [B17] after this step.
- Enter the nominal operating frequency F_S [B22]. (F_S is the normal operating frequency when the power supply is operating at normal peak output power point with nominal component values.) Note: Recommended frequency is between 70 kHz and 85 kHz.
- Enter V_{DS} [B24], the on-state drain source voltage drop. Use 10 V if no better data is available.
- Enter the output rectifier's forward voltage drop V_D [B25]. Use 0.5 for Schottky and 0.7 for standard PN-junction diodes.
- Verify that K_P [D26] is greater than 1.0 to ensure discontinuous operation. For better CC tolerance set a value for K_P greater than 1.15.
- Enter the feedback winding turns in [B30]; it has to make sure the V_{FLY} [B31] is higher than 4 V.
- Enter the bias winding voltage VB [B36], 10 V is recommended to minimize no-load input power. Note: If the V_{FLY} [B30] is higher than 10 V, the feedback winding can be shared as a bias winding, separate bias winding is not necessary.
- Enter 4.6 μs for D_{CON} [B40], the output rectifier's conduction time. Note: The D_{CON} is the desired value, the D_{CON_FINAL} is the real D_{CON} assuming integer value for N_P, N_S and V_{MIN}.
- Enter the core type from the drop-down menu [B48]. If the desired core is not listed, select "Custom" from the drop-down menu, and manually enter the core name in Custom-Core [B49], then you may enter a core's characteristics A_E, L_E and A_L ([B51] [B52] [B53]).

Output Power Table[1,2,3,4]

Product[5]	90-264 VAC	
	D (SO-8C) Package	
	Adapter	Open Frame
LNK6404D / LNK6424D	3.5 W	4.1 W
LNK6405D / LNK6415D / LNK6425D	4.5 W	5.1 W
LNK6406D / LNK6416D / LNK6426D / LNK6436D / LNK6446D	5.5 W	6.1 W
LNK6407D / LNK6417D / LNK6427D	7.5 W	7.5 W
Product[5]	**E (eSIP-7C) and K (eSOP-12B) Packages**	
	Adapter	**Open Frame**
LNK6407K / LNK6417K / LNK6427K	8.5 W	9 W
LNK6408K / LNK6418K / LNK6428K / LNK6448K	10 W	10 W
LNK6408E / LNK6418E / LNK6428E / LNK6448E	10 W	10 W

Table 1. Output Power Table.

Notes:
1. Assumes minimum input DC voltage >90 VDC, K_P ≥1 (Recommend K_P ≥1.15 for accurate CC regulation), η >78%, D_{MAX} <55%.
2. Output power capability is reduced if a lower input voltage is used.
3. Minimum continuous power with adequate heat sink measured at 50 °C ambient with device junction below 110 °C.
4. Assumes bias winding is used to supply BYPASS pin.
5. Package: D: SO-8C, E: eSIP-7C, K: eSOP-12B.

- Enter the bobbin width BW [B54].
- Enter the margin tape width in [B55], if margin tape is desired. Note: This reduces the winding width by twice the entered value.
- Enter the number of primary layers L [B56]. Use a maximum of 3 layers to limit the primary leakage inductance value.
- Enter the primary inductance tolerance $L_{P(TOLERANCE)}$ [B73].
- Enter in the transformer's core maximum flux density $B_{M(TARGET)}$ [B76]. Note: Use no more than the max flux density, 2600 Gauss, to keep the transformer's audible noise to acceptable levels. Follow the guidance in column F to address any warnings.
- Verify that the core's gap L_G [D81], the wire gauge AWG [D86], and the primary's winding current density CMA [D87] are within acceptable limits.
- Verify that the LinkSwitch-3 drain voltage [D99] is less than 680 V.
- Use resistor values R_{UPPER} [D43] and R_{LOWER} [D44] for feedback resistors (Figure 1).
- Using PIVs [D100] and I_{SRMS} [D93] determine the proper output rectifier.
- Select the input capacitor voltage rating to be above V_{MAX} [D61], and select the ripple current rating to be above I_{RIPPLE} [D67].
- Using V_O [B8], ISP [D90], and I_{RIPPLE} [D94], determine the proper output filter capacitor.
- Using I_{AVG} [D65] and an estimated peak reverse voltage of 600 V to 1000 V, determine the input rectifier diodes (typically 1N4006 or 1N4007 types).
- Using I_{AVG} [D65] determine the proper input filter inductor current rating. Usually an inductor value of 1 mH to 2 mH is adequate to meet conducted EMI requirements.
- After building the prototype power supply, measure the output voltage and current at the peak power point. Enter the values used for R_{UPPER} and R_{LOWER} in cells [B103] and [B104], respectively.

- Enter the measured voltage in cell [B105]. Enter the measured current at the transition from CV to CC operation in cell [B106]. PIXls calculates the fine-tuned feedback resistors' values for the power supply. Install the closest 1% value resistors for R_{UPPER} [D107] and RL_{OWER} [D108].

Step-by-Step Design Procedure

Step 1 – Enter Application Variables VAC_{MIN}, VAC_{MAX}, f_L, V_O, I_O, h, Z, V_B, t_C, Bias Support, C_{IN}

Determine the input voltage range from Table 2.

Note: For designs that have a DC rather than an AC input, enter the values for minimum and maximum DC input voltages, V_{MIN} [B60] and V_{MAX} [B61], directly into the grey override cell on the design spreadsheet (see Figure 6).

Line Frequency, F_L
Typical line frequencies are 50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC, and 50 Hz for single 230 VAC inputs. These values represent typical, rather than minimum, frequencies. For most applications this gives adequate overall design margin. To design for the absolute worst case, or based on the product specifications, reduce these numbers by 6% (to 47 Hz or 56 Hz). For half-wave rectification use $F_L/2$. For DC input enter the voltage directly into cells [B60] and [B61].

Nominal Output Voltage, V_O (V)
For both CV/CC and CV-only designs V_O is the nominal output voltage measured at the end of an attached cable carrying nominal output current. The tolerance for the output voltage is ±5% (including initial tolerance and over the data sheet specified junction temperature range).

Minimum Required Output Current, I_O (A)
For CV/CC designs I_O is the minimum required output current at nominal output voltage.

The nominal output voltage and current may not be the same as the name-plate specification in the case of an external adapter. Typically the nameplate specification represents the minimum output voltage and current of the adapter, ensuring that when measured, the adapter delivers at least $V_{O(MIN)}$ and $I_{O(MIN)}$, to satisfy energy-efficiency measurement-test methods. Refer to Figure 3 for definitions of output voltage and current.

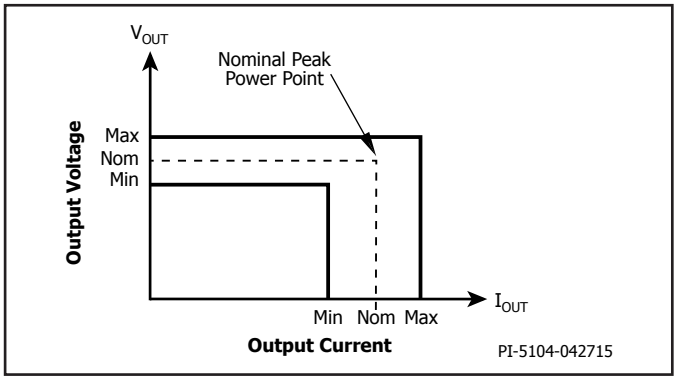

Figure 2. Output Characteristic Envelope Definitions.

Nominal Input Voltage (VAC)	VAC_{MIN}	VAC_{MAX}
100/115	85	132
230	195	265
Universal	85	265

Table 2. Standard Worldwide Input Line Voltage Ranges.

For example, if the nominal CC level is 2.2 A, then the minimum I_O is 1.98 A, and the maximum I_O is 2.42 A with 10% tolerance. Then 1.98 A should be input for minimum required current I_O.

Power Supply Efficiency, η
Enter the estimated efficiency of the complete power supply: measure voltage and current at the end of the output cable (if applicable) under full load conditions and worst-case line (generally lowest input voltage). Start with 0.76 for universal input (85-265 VAC) or single 100/115 VAC (85-132 VAC) input voltage and 0.78 for a single 230 VAC (185-265 VAC) input voltage design.) Adjust the number accordingly after measuring the efficiency of the first prototype-board at the peak output power point, and at both VAC_{MIN} and VAC_{MAX}.

ENTER APPLICATION VARIABLES				Design Title
VACMIN		90.00	V	Minimum AC Input Voltage
VACMAX		265.00	V	Maximum AC Input Voltage
fL		50.00	Hz	AC Mains Frequency
Application Type	**Open Frame**	Open Frame		Choose application type
VO		5.00	V	Output Voltage (at continuous power)
IO		0.75	A	Minimum required output current
Power		3.75	W	Continuous Output Power
n		0.75		Efficiency Estimate at output terminals.
Z		0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC		3.00	ms	Bridge Rectifier Conduction Time Estimate
CIN	30.00	30.00	uF	Input Capacitance

Figure 3. Application Variables Section of the Design Spreadsheet.

DC INPUT VOLTAGE PARAMETERS				
VMIN		117.76	V	Minimum DC bus voltage
VMAX		374.77	V	Maximum DC bus voltage

Figure 4. DC Input Voltage Parameters Section of the Design Spreadsheet.

Power Supply Loss Allocation Factor, Z
This factor represents the ratio of power loss from the secondary relative to the total power loss from both the primary and secondary in the power supply. Z is used with the calculated efficiency to determine the actual power the power stage must deliver. For example, losses in the input stage (EMI filter, rectification, etc.) are not processed by the power stage (transferred through the transformer). Therefore, although they reduce efficiency, the transformer design is not impacted.

$$Z = \frac{\text{Secondary Side Losses}}{\text{Total Losses}}$$

Use a value of 0.5 if no other data is available.

Bridge Diode Conduction Time, t_C (ms)
This is the duration of the incoming AC sine wave during which the input diodes conduct, charging the input capacitance. This value is used in the calculation of the minimum voltage across the input capacitance at $V_{AC(MIN)}$. The actual value for t_C can be found by measuring the input current waveform on a prototype. Use a value of 3 ms if no other data is available.

Total Input Capacitance, C_{IN} (μF)
Enter total input capacitance using Table 3 for guidance. The capacitance is used to calculate the minimum voltage, V_{MIN}, across the bulk capacitor. Select a value for C_{IN} that keeps V_{MIN} >90 V.

Total Input Capacitance per Watt Output Power (μF/W)	
AC Input Voltage (VAC)	**Full Wave Rectification**
100/115	2.5
230	1
85-265	2.5

Table 3. Suggested Total Input Capacitance for Different Input Voltage Ranges.

Step 2 – Enter LinkSwitch-3 Variables: LinkSwitch-3 Device and Package, VDS and VD

Output Power Table[1,2,3,4]

Product[5]	90-264 VAC	
	D (SO-8C) Package	
	Adapter	Open Frame
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LNK6407D / LNK6417D / LNK6427D	7.5 W	7.5 W
Product[5]	**E (eSIP-7C) and K (eSOP-12B) Packages**	
	Adapter	**Open Frame**
LNK6407K / LNK6417K / LNK6427K	8.5 W	9 W
LNK6408K / LNK6418K / LNK6428K / LNK6448K	10 W	10 W
LNK6408E / LNK6418E / LNK6428E / LNK6448E	10 W	10 W

Table 4. Output Power Table.

Select the correct LinkSwitch-3 device and package. Refer to the LinkSwitch-3 power table (Table 4) and select a device for the desired output power and operating conditions (sealed adapter or open frame). Type D package for the 7-pin surface mount S0-8C, K package for the 11-pin surface mount eSOP-12B (LNK64x7 and LNK64x8) or E package for the 6-pin through hole eSIP-7C (LNK64x8 only). (See Figure 5 for this and the next four steps).

Select the Cable Drop Compensation option
Select the cable compensation option (Table 5) to most closely match the percentage output voltage drop in the output cable. For example, a 5 V, 2 A LNK64x8K design with a cable impedance of 150 MΩ has a cable voltage drop of -0.3 V. With a desired nominal output voltage of 5 V (at the end of the cable) this represents a voltage drop of 6%. In this case, select the +6% compensation, to give the smallest error. The complete part number will be showed in [B18] after this step.

LinkSwitch-3 Output Cable Voltage Drop Compensation	
Device	**Output Voltage Change Factor (±1%)**
LNK640x	1.02
LNK641x	1.04
LNK642x	1.06
LNK643x	1.08
LNK644x	1.01

Table 2. Cable Compensation Change Factor vs. Device.

Select the Operating Frequency, F_S
Enter the nominal operating switching frequency F_S. F_S is the switching frequency when the power supply is operating at the nominal peak output power point. Select a frequency range between 70 kHz and 85 kHz. The minimum and maximum frequency in operation varies depending on the tolerance of L_P and the internal current limit. A warning will be displayed should the calculated minimum or maximum frequency be outside the range of 45 kHz to 100 kHz.

LinkSwitch-3 ON-State Drain-to-Source Voltage, V_{DS} (V)
This parameter is the average ON-state voltage developed across the LinkSwitch-3 DRAIN and SOURCE pins. If no value is entered, the PIXls uses a default value of 10 V.

Output Diode Forward-Voltage Drop, V_D (V)
Enter the average forward-voltage drop of the output diode. Use 0.5 V for a Schottky diode or 0.7 V for a PN-junction diode (if specific diode data is not available). V_D has a default value of 0.5 V.

Ratio of MOSFET Off Time to Secondary Diode Conduction Time, K_P
For proper regulation, LinkSwitch-3 requires the power supply to operate in discontinuous conduction mode. Verify that K_P is greater than 1.0 to ensure discontinuous operation. For better CC tolerance, set a value for K_P greater than 1.15 (15% margin taken into account the frequency jitter, component tolerance, ect.). K_P should always be greater than 1, indicating discontinuous conduction mode, and is the ratio of primary MOSFET off time to the secondary diode conduction time.

$$K_P \equiv K_{DP} = \frac{(1-D)\times T}{t} = \frac{V_{OR}\times(1-D_{MAX})}{(V_{MIN}-V_{DS})\times D_{MAX}}$$

Feedback Winding Parameter
The Feedback Winding Parameters are calculated by the PIXls spreadsheet. N_{FB} is the number of feedback winding turns in the transformer. V_{FLY} and V_{FOR} represent the voltage across the feedback winding while the MOSFET is on (V_{FOR}) or off (V_{FLY}).

Bias Winding Parameters – Choose External Bias
Select external bias if an external bias supply for LinkSwitch-3 is required and a bias winding should be added to the trans-former. External bias support increases efficiency, especially at light load, and lowers no-load input power consumption by disabling the internal high-voltage supply for the IC. For LNK64X7, LNK64X8, an external bias is mandatory as the internal shunt (self-bias) current is not enough to supply the IC current during full load.

If a feedback winding voltage (V_{FLY}) is equal or higher than 10 V, bias winding can be the same as feedback winding. If the feedback winding voltage (V_{FLY}) is lower than 10 V, enter the bias voltage for V_B (Figure 7). Use 10 V to minimize no-load input power.

N_B is the number of bias winding turns. R_{EXT} is the resistor between the bias winding output diode to the BYPASS pin.

Step 3 – Select Output Diode Conduction Time, D_{CON} (ms)

D_{CON} is a preset value, the D_{CON_FINAL} is the final D_{CON} value recalculated with the integrated N_S (Secondary winding turns) and N_P (primary winding turns). D_{CON_FINAL} is the output diode conduction time at the peak output power point. Changing the value for D_{CON} (Eventually D_{CON_FINAL}) can be used to adjust the number of secondary and feedback winding turns for better bobbin winding window coverage. Increasing D_{CON} (Eventually D_{CON_FINAL}) increases the number of turns.

The minimum value for D_{CON} is limited to 4.6 µs at full load to ensure that under light loads when the feedback winding is sampled, after the internal MOSFET is turned off, the output diode is still conducting. The maximum value of D_{CON} is normally limited by the value of K_P. As D_{CON} increases, K_P decreases until it reaches its minimum value of 1.0. Resistors R_{UPPER} and R_{LOWER} are the calculated initial values for the feedback winding resistors.

Step 4 – Choose Core and Bobbin Based on Output Power and Enter A_E, L_E, A_L, B_W, L

These symbols represent core effective cross-sectional area A_E (cm^2), core effective path length L_E (cm), core ungapped effective inductance A_L ($nH/Turn^2$), bobbin width B_W (mm) and number of primary layers L.

By default, if the Core cell is left empty, the spreadsheet selects the smallest core size that meets the peak flux density limit. The user can change this selection and choose an alternate core from a list of commonly available cores (shown in Table 6). Table 6 provides guidance on the power capability of specific core sizes.

The gray override cells [B51] through [B56] can be used to enter the core and bobbin parameters directly. This is useful for either selecting a core that is not on the list, or if the specific core or bobbin information differs from that recalled by the spreadsheet.

ENTER LinkSwitch-3 VARIABLES					
Chosen Device	**LNK64x8E**	LNK64x8E		Chosen LinkSwitch-3 device and package. E.g. - LNK64x4D or LNK64x8K	Chosen LinkSwitch-3 device and package. E.g. - LNK64x4D or LNK64x8K
Cable drop compensation option	**No comp**	No comp		Select level of cable drop compensation	Select level of cable drop compensation
Complete Part Number		LNK6448E		Full Part Number	Full Part Number
ILIMITMIN		0.47	A	Minimum Current Limit	Minimum Current Limit
ILIMITTYP		0.50	A	Typical Current Limit	Typical Current Limit
ILIMITMAX		0.54	A	Maximum Current Limit	Maximum Current Limit
FS		80.00	kHz	Typical Device Switching Frequency at maximum power	Typical Device Switching Frequency at maximum power
VOR		39.29	V	Reflected Output Voltage (VOR < 135 V Recommended)	Reflected Output Voltage (VOR < 135 V Recommended)
VDS		10.00	V	LinkSwitch-3 on-state Drain to Source Voltage	LinkSwitch-3 on-state Drain to Source Voltage
VD		0.50	V	Output Winding Diode Forward Voltage Drop	Output Winding Diode Forward Voltage Drop
KP		1.72		KP assuming minimum LP, VMIN, and Maximum Switching Frequency, but not including frequency jitter.	KP assuming minimum LP, VMIN, and Maximum Switching Frequency, but not including frequency jitter.

Figure 5. Enter LinkSwitch-3 Variables of the Design Spreadsheet.

FEEDBACK WINDING PARAMETERS				
NFB	10.00	10.00		Feedback winding turns
VFLY		6.88	V	Flyback Voltage - Voltage on Feedback Winding during switch off time
VFOR		11.11	V	Forward voltage - Voltage on Feedback Winding during switch on time

Figure 6. Feedback Winding Parameters Section of the Design Spreadsheet.

BIAS WINDING PARAMETERS				
BIAS	**Ext. Bias**	Ext. Bias		Select between self bias or external bias to supply the IC. Note that this will affect ILIMIT
VB		10.00	V	Bias Winding Voltage. Ensure that VB > VFLY. Bias winding is assumed to be AC-STACKED on top of Feedback winding
NB		6.00		Bias Winding number of turns
REXT		7.50	k-ohm	Suggested value of BYPASS pin resistor (use standard 5% resistor)

Figure 7. Bias Winding Parameters Section of the Design Spreadsheet.

For designs that require safety isolation between primary and secondary but are not using triple insulated wire, enter the width of the safety margin to be used on each side of the bobbin as parameter M. Universal input designs typically require a total margin of 6.2 mm, and a value of 3.1 mm entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical. However, for a total required margin of 6.2 mm (for example), enter 3.1 mm even if the physical margin is only on one side of the bobbin.

Core Size	Output Power Capability
EF12.6	3.3 W
EE13	3.3 W
EE16	6.1 W
EF20	10 W

Table 6. Output Power Capability of Commonly used Sizes in LinkSwitch-3 Designs.

For designs using triple-insulated wire it may still be necessary to enter a small margin to meet required safety creepage distances. Typically many bobbins exist for each core size, each with different mechanical spacing. Refer to the bobbin data sheet or seek guidance from your safety expert or transformer vendor, to determine the requirement for your design. The margin reduces the available area for windings, so margin construction may not be suitable for transformers with smaller cores. If, after entering the margin, more than three primary layers (L) are required, either select a larger core or switch to a zero-margin design using triple-insulated wire.

Transformer Core Size	
EE8	EFD20
EE10	EFD25
EE12.9	EPC13
EE13	EPC17
EE16	EPC19
EE16W	EI16
EE1616	EI19
EE19	EI22
EE22	EI25
EEM12.4	EEL16
EF12.6	EEL19
EF16	EEL22
EF20	RM5
EFD1C	RM5/I
EFD12	RM6S
EFD15	RM6S/I

Table 7. List of Cores Provided in LinkSwitch-3 PIXls Spreadsheet.

Enter the number of primary layers (L). The maximum number of recommended primary layers is three. A larger number of layers increase leakage inductance, which increases losses.

DESIGN PARAMETERS				
DCON	5.10	5.10	us	Desired output diode conduction time
DCON_FINAL		5.24	us	Final output conduction diode, assuming integer values for NP and NS, and VMIN
TON		3.24	us	LinkSwitch-3 On-time (calculated at LPMIN, VMIN and ILIMITMIN)
RUPPER		30.97	k-ohm	Upper resistor in Feedback resistor divider
RLOWER		12.18	k-ohm	Lower resistor in resistor divider

Figure 8. Design Parameters Section of the Design Spreadsheet.

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Core Type				
Core	**Auto**	EE13		Enter Transformer Core.
Custom_Core				Enter Core name if selection on drop down menu is "Custom"
Bobbin		BE-13		Bobbin part number
AE		17.10	mm^2	Core Effective Cross Sectional Area
LE		30.20	mm	Core Effective Path Length
AL		1130.00	nH/turn^2	Ungapped Core Effective Inductance
BW		7.40	mm	Bobbin Physical Winding Width
M		0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L		3.00		Number of Primary Layers
NS		8.00	turns	Number of Secondary Turns. To adjust Secondary number of turns change DCON

Figure 9. Enter Transformer Core/Construction Variables.

TRANSFORMER SECONDARY DESIGN PARAMETERS				
ISP		3.09	A	Peak Secondary Current assuming Ilimitmin
ISRMS		1.47	A	Secondary RMS Current assuming Ilimitmax and Dmax
IRIPPLE		1.26	A	Output Capacitor RMS Ripple Current
CMS		293.25	Cmils	Secondary Bare Conductor minimum circular mils
AWGS		25.00		Secondary Wire Gauge (Rounded up to next larger standard AWG value)

Figure 10. Transformer Secondary Design Parameters Section of the Design Spreadsheet.

VOLTAGE STRESS PARAMETERS				
VDRAIN		547.80	V	Maximum Drain Voltage Estimate (Assumes 20% clamping voltage tolerance and an additional 10% temperature tolerance)
PIVS		33.28	V	Output Rectifier Maximum Peak Inverse Voltage

Figure 11. Voltage Stress Parameters Section of the Design Spreadsheet.

FINE TUNING				
RUPPER_ACTUAL		30.97	k-ohm	Actual Value of upper resistor (RUPPER) used on PCB
RLOWER_ACTUAL		12.18	k-ohm	Actual Value of lower resistor (RLOWER) used on PCB
Actual (Measued) Output Voltage (VDC)		5.00	V	Measured Output voltage from first prototype
Actual (Measured) Output Current (ADC)		0.75	Amps	Measured Output current from first prototype
RUPPER_FINE		30.97	k-ohm	New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 30.9 k-ohms
RLOWER_FINE		12.18	k-ohm	New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 12.1 k-ohms

Figure 12. Fine Tuning Section of the Design Spreadsheet.

DC INPUT VOLTAGE PARAMETERS				
VMIN		117.76	V	Minimum DC bus voltage
VMAX		374.77	V	Maximum DC bus voltage

Figure 13. DC Input Voltage Parameters Section of the Design Spreadsheet.

CURRENT WAVEFORM SHAPE PARAMETERS				
DMAX		0.32		Maximum duty cycle measured at VMIN
IAVG		0.05	A	Input Average current, at VMIN
IP		0.23	A	Peak primary current
IR		0.23	A	Primary ripple current
IRMS		0.09	A	Primary RMS current

Figure 14. Current Waveform Shape Parameters Section of the Design Spreadsheet.

TRANSFORMER PRIMARY DESIGN PARAMETERS				
LPMIN		1638.00	uH	Minimum Primary Inductance
LPTYP		1820.00	uH	Typical Primary inductance
LP_TOLERANCE		10.00	%	Tolerance in primary inductance
NP		106.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
ALG		161.98	nH/turn^2	Gapped Core Effective Inductance
BM_TARGET	2500.00	2500.00	Gauss	Target Flux Density
BM		2510.21	Gauss	Maximum Operating Flux Density (calculated with LPTYP, ILIMITTYP), BM < 2600 is recommended
BP		2948.99	Gauss	Peak Operating Flux Density (calculated with LPMAX, ILIMITMAX), BP < 3100 is recommended
BAC		1255.10	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		158.81		Relative Permeability of Ungapped Core
LG		0.13	mm	Gap Length (LG > 0.1 mm)
BWE		22.20	mm	Effective Bobbin Width
OD		0.21	mm	Maximum Primary Wire Diameter including insulation
INS		0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.17	mm	Bare conductor diameter
AWG		34	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		40.32	Cmils	Bare conductor effective area in circular mils
CMA		463.14	Cmils/A	Primary Winding Current Capacity (200 < CMA < 500)

Figure 15. Transformer Primary Design Parameters Section of the Design Spreadsheet.

N_S is the number of secondary turns. To increase the number of turns, increase the value of D_{CON} [B40].

Step 5 – Iterate Transformer Design and Generate Key Transformer Design Parameters

Iterate the design, making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column. Messages marked "!!! Info" provide guidance for acceptable parameters that can be further optimized. Once all warnings have been cleared, use the transformer design parameters to either wind a prototype transformer, or to send to a vendor for obtaining samples.

Primary Inductance, $L_{P(TYP)}$, $L_{P(MIN)}$ (mH), $L_{P(TOLERANCE)}$, (%)
The key transformer electrical parameters are $L_{P(TYP)}$, $L_{P(MIN)}$ (mH), $L_{P(TOLERANCE)}$ and represents the minimum primary inductance needed to deliver the nominal peak output power ($V_O \times I_O$). As it is more common to specify the primary inductance to a vendor as a nominal value with tolerance, the value for $L_{P(TYP)}$ is calculated via the expression:

$$L_{P(TYP)} = L_{P(MIN)} \times \left(1 + \frac{L_{P(TOLERANCE)}}{100}\right)$$

where $L_{P(TOLERANCE)}$ is the entered percentage tolerance. If no value is entered, PIXls uses 10 by default, signifying $L_{P(TOLERANCE)}$ of ±10%.

The expression used to calculate $L_{P(MIN)}$ includes the output cable voltage drop via the entered value for efficiency and Z factor.

Primary Winding Number of Turns, N_P
This is the total number of primary winding turns.

Gapped Core Effective Inductance, A_{LG} (nH/T²)
This is the target core effective inductance at $L_{P(MIN)}$ for the typical A_{LG} value multiplied by $1+(L_{P(TOLERANCE)/100})$. This value is typically used by transformer vendors to purchase the cores with the correct gap size.

Target Flux Density, B_{M_TARGET} (Gauss)
B_{M_TARGET} is the operating core flux density and the AC flux swing. Use a maximum value of 2600 (0.26 T) to minimize audible noise generation.

Core Gap Length, L_G (mm)
L_G is the estimated core gap length. Values below 0.1 mm are generally not recommended for center-leg gapped cores due to the resultant increase in primary inductance tolerance. If you require such a low value, consult with your transformer vendor for guidance.

Maximum Primary Winding Wire Outside Diameter, OD (mm)
This is the calculated maximum outside wire diameter to allow the primary winding to fit into the number of specified layers. When selecting the wire type use double-coated magnetic wire (rather than single-coated types) for improved reliability and reduced primary capacitance (lower no-load input power).

Primary Winding Wire Bare Conductor Diameter, DIA (mm)

Primary Winding Wire Gauge, AWG
This is the calculated conductor diameter rounded to the next smallest standard American Wire Gauge size.

Primary Winding Bare Conductor Effective Area, CM(C_{MILS})
CM is the effective conductor area in circular mils.

Primary Winding Wire Current Capacity, CMA (C_{MILS}/A)
CMA is the primary conductor area in circular mils (where 1 mil = 1/1000th of inch) per Amp. Values below the recommended minimum of 200 maybe acceptable if worst-case winding temperature is verified.

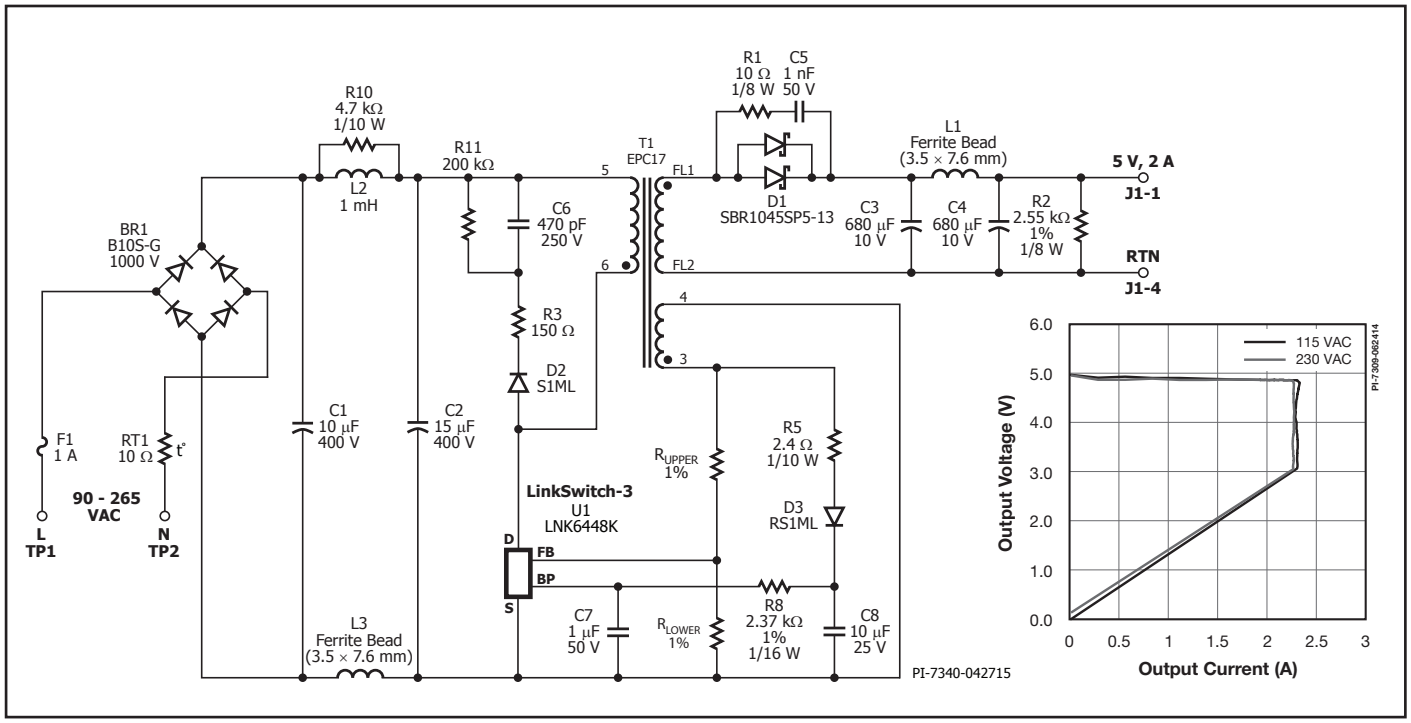


Figure 16. Energy Efficient USB Charger Power Supply (78% Average Efficiency, <30 mW No-load Input Power).

Step 6 – Selection of Input Stage

The recommended input stage is shown in Table 8. It consists of a fusible element, input rectification, and line filter network.

The fusible element can be either a fusible resistor or a fuse. If a fusible resistor is selected, use a flameproof type.

Depending on the differential line input surge requirements, a wire-wound type may be required. Avoid using metal or carbon film types as these can fail due to the inrush current when VAC_{MAX} is applied repeatedly to the supply.

In designs using a Y capacitor, place the EMI filter inductor on the opposite side of the input to the Y capacitor connection. For example, place the input inductor (L_{IN1}) between the negative terminals of the input capacitors (C_{IN1} and C_{IN2}) where the Y capacitor returns to the DC rail (see Figure 33).

Conducted EMI filtering is provided by L_{IN1} and L_{IN2}, which together with C_{IN1} and C_{IN2}, form a pi (π) filter. A single inductor is suitable for designs below 3 W or where EMI is measured with the output of the supply floating (i.e. not connected to safety earth ground). Although two inductors are generally required above 3 W, a ferrite bead may be sufficient, especially where the output of the supply is floating.

Normally the total input capacitance is divided equally between the two input capacitors (C_{IN1} and C_{IN2}). However, for lower cost, two different capacitance values may be used. In this case, select C_{IN1} as ≥1 μF (or as needed) to prevent overvoltage of the capacitor during differential mode surge. Select the second capacitor C_{IN2} to meet both an overall capacitance (C_{IN1} + C_{IN2}) of 2.5 μF/W of output power, and 3 μF/W of output power for highest low-line efficiency with universal input voltage.

Differential mode EMI generation is a strong function of the equivalent series resistance (ESR) of C_{IN2}, as this capacitor supplies the primary switching current. Selecting a lower ESR capacitor series for C_{IN2} than C_{IN1} can help reduce differential mode (low frequency) conducted EMI while optimizing the overall cost of the two capacitors.

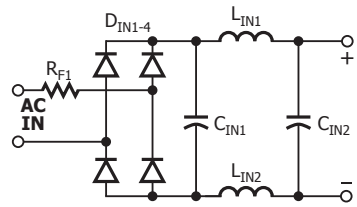
Table 8 shows the input filter schematic, gives a formula for selecting C_{IN1} + C_{IN2}, and tells how to adjust the input capacitance for other input voltage ranges.

Step 7 – Selection of BYPASS Pin Capacitor, Bias Winding and Feedback Components

Use a 1 μF BYPASS pin capacitor (C7 in figure 16) with a voltage rating greater than 7 V. The capacitor must be physically located close to the LinkSwitch-3 BYPASS pin.

Bias Winding Components

A bias winding is required when using LNK64x7 and LNK64x8, as the internal shunt output current is not enough to supply the necessary IC current during full load. A bias winding is optional for LNK64x4 to LNK64x6. The addition of a bias circuit decreases the no-load input power from ~200 mW down to less than 30 mW. This increases efficiencies at lighter loads enough to allow using cost-reducing options while still meeting average efficiency requirements. A PN-junction diode may replace a higher-cost Schottky-barrier diode, or the output cable may be replaced by one constructed of smaller diameter wire (higher impedance).



R_{F1}: 8.2 Ω, 1 W, Fusible, flameproof
L_{IN1}: 470 μH – 2.2 mH, 0.05 A – 0.3 A
L_{IN2}: Ferrite bead or 470 μH – 2.2 mH, 0.05 A – 0.3 A
C_{IN1} + C_{IN2}: ≥ 2.5 μF/W_{OUT}, 400 V, 85 VAC - 265 VAC
: ≥ 2.5 μF/W_{OUT}, 200 V, 100 VAC - 115 VAC
: ≥ 1 μF/W_{OUT}, 400 V, 185 VAC - 265 VAC
D_{INX}: 1N4007, 1 A, 1000 V

Table 8. Input Stage Recommendation.

The power supply schematic shown in Figure 16 uses the bias circuit. Diode D3, capacitor C8, and resistor R8 form the bias circuit. If the feedback winding voltage (V_{FLY} in the design spreadsheet) is >10 V, an additional winding for the bias winding is not required. The bias winding shares the same winding with the feedback winding. If the output voltage is less than 9 V, then an additional transformer winding is needed, AC-stacked on top of the feedback winding. This provides a high enough voltage to supply the BYPASS pin even during low switching frequency operation at no-load.

Figure 17 shows an example of the additional bias winding (from pin 3 to pin 2) stacked on top of the feedback winding (pin 4 to pin 3). Diode D3 rectifies the output and C8 is the filter capacitor. A 10 μF capacitor is recommended to hold up the bias voltage during the low frequency operation at no-load. The capacitor type is not critical but its voltage rating should be above the maximum value of V_{BIAS}. The recommended current into the BYPASS pin is equal to the IC supply current (~0.48 mA to 0.7 mA depending on the size). The value of R4 is calculated according to

$$(V_{BIAS} - V_{BP})/I_{S2}$$

where V_{BIAS} (10 V typical) is the voltage across C8, I_{S2} (0.48 mA to 0.7 mA depending on the size) is the IC supply current, and V_{BP} (6.4 V typical) is the BYPASS pin voltage. The parameters I_{S2} and V_{BP} are provided in the parameter table of the LinkSwitch-3 data sheet. The BYPASS pin current should not exceed 10 mA at the maximum bias winding voltage (normally when the output voltage is fully loaded). With a fixed pre load resistor, the no-load power consumption will be changed if the resistor (R4) in the bias winding changes. Lower R4 resistor value will cause higher no-load power consumption as it causes higher bias winding energy consumption at no-load. Too low R4 resistor value has to be avoided too, as it decreases the energy dissipation ratio between the main output and the bias winding at no-load that may cause worse output voltage regulation.

Diode D3 can be any low-cost diode such as FR102, 1N4148, or BAV19/20/21. The diode voltage stress is given in the Bias Winding Parameter section of the design spreadsheet.

FEEDBACK Pin Resistor Values, Initial Values

Resistors R_{UPPER} and R_{LOWER} form a resistor divider network that sets the voltage on the FEEDBACK (FB) pin during both the on-time and off-time of the internal MOSFET.

During CV operation the controller regulates the FEEDBACK pin voltage to remain at V_{FBth} using an ON/OFF state-machine. The FEEDBACK pin voltage is sampled 2.5 µs at full load after the turn-off of the internal MOSFET. At light loads the current limit reduces to decrease the transformer flux density and the FEEDBACK pin voltage will be sampled earlier than 2.5 µs.

During CC operation the switching frequency is adjusted as the FEEDBACK pin voltage changes, to provide constant output current regulation.

During the MOSFET on-time the FEEDBACK pin voltage is used to monitor the DC input voltage and thereby minimize CC variation across the input line range.

The initial values of R_{UPPER} and R_{LOWER} are provided in cells [D43] and [D44], for uses in the initial prototype build. Once a prototype has been built and tested follow the fine-tuning procedure described below to determine the final resistor values. Use the closest 1% values for best results. Place R_{UPPER} and R_{LOWER} as close to the FEEDBACK pin as possible.

Fine-Tuning

Enter the fine-tuning values into the Fine-Tuning section of the design spreadsheet (Figure 12) after building a prototype power supply. Enter the actual values used for feedback resistors R_{UPPER} and R_{LOWER} in cells [D101] and [D102], and the measured power supply output voltage and current at the peak output power point in cells [D103] and [D104]. The PIXls spreadsheet will calculate the refined feedback resistor values for $R_{UPPER(FINE)}$ and $R_{LOWER(FINE)}$ to center both the output voltage and current.

Step 8 – Selection of Output Diode and Pre-Load

The output rectifier diode should be either a fast or an ultrafast recovery PN junction or Schottky-barrier type.

Select a diode with sufficient margin to the specified voltage rating (V_R). Typically $V_R \geq 1.2 \times$ PIVs, where PIVs is taken from the Voltage Stress Parameters section of the spreadsheet. Once a prototype is completed use an oscilloscope to measure the actual diode stress at VAC_{MAX}.

Select the diode with the closest rating to $I_D \geq 2 \times I_O$, where I_D is the diode's rated current and I_O is the output current. Take the diode's self-heating into consideration and use a larger diode, if needed, to meet thermal or efficiency requirements. Table 9 lists some of the suitable Schottky and ultrafast diodes that may be used with LinkSwitch-3 circuits.

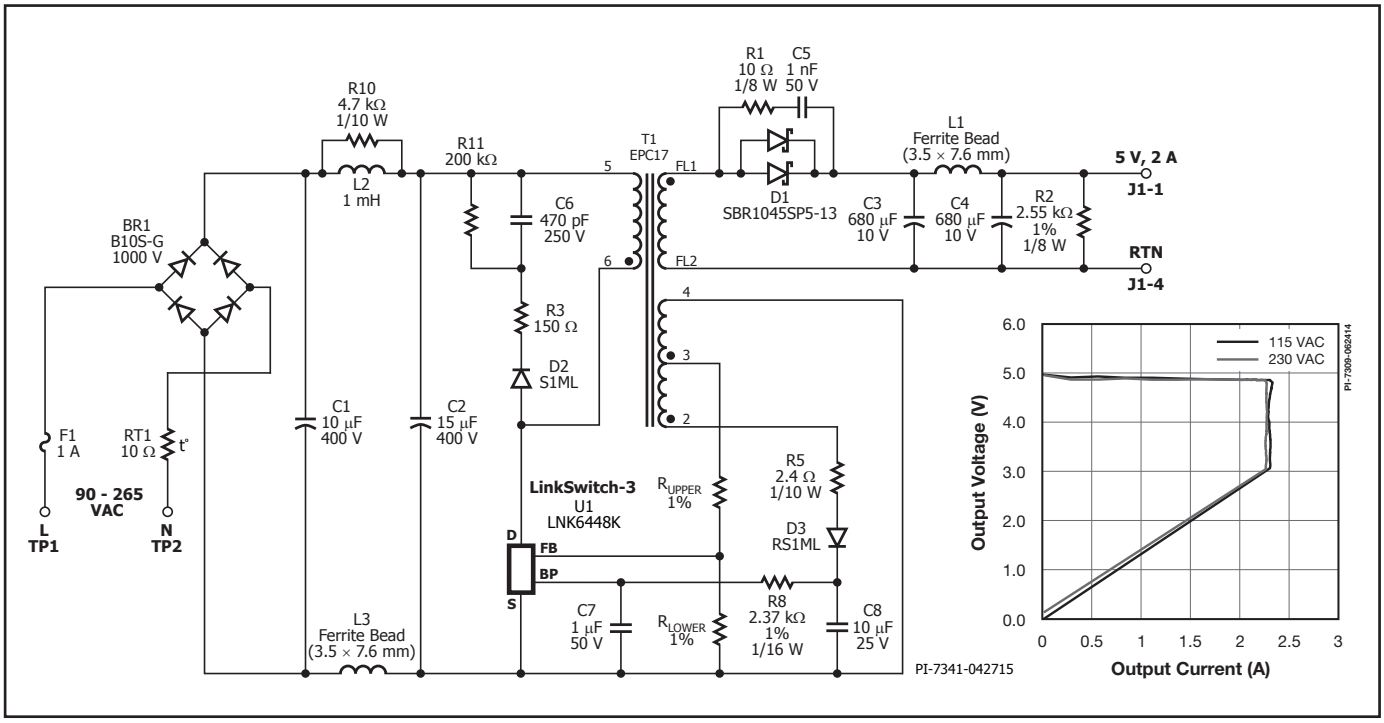


Figure 17. Energy Efficient USB Charger Power Supply (78% Average Efficiency, <30 mW No-load Input Power) (Bias Winding is AC Stack on Top of Feedback Winding).

Series Number	Type	VR Range	I_F	Package	Manufacturer
		V	A		
1N5817 to 1N5819	Schottky	20-40	1	Leaded	Vishay
SB120 to SB1100	Schottky	20-100	1	Leaded	Vishay
11DQ50 to 11DQ60	Schottky	50-60	1	Leaded	Vishay
1N5820 to 1N5822	Schottky	20-40	3	Leaded	Vishay
MBR320 to MBR360	Schottky	20-60	3	Leaded	Vishay
SB320 to SB360	Schottky	20-60	3	Leaded	Vishay
SB520 to SB560	Schottky	20-60	5	Leaded	Vishay
MBR1045	Schottky	35/45	10	Leaded	Vishay
UF4002 to UF4006	Ultrafast	100-600	1	Leaded	Vishay
UF5401 to UF5408	Ultrafast	100-800	3	Leaded	Vishay
MUR820 to MUR860	Ultrafast	200-600	8	Leaded	Vishay
BYW29-50 to BYW29-300	Ultrafast	50-200	8	Leaded/SMD	Vishay
ESA1A to ES1D	Ultrafast	50-200	1	SMD	Vishay
ES2A to ES2D	Ultrafast	50-200	2	SMD	Vishay
SL12 to SL23	Schottky (low V_F)	20-30	1	SMD	Vishay
SL22 to SL23	Schottky (low V_F)	20-30	2	SMD	Vishay
SL42 to SL44	Schottky (low V_F)	20-30	4	SMD	Vishay
SBR1045SD1	Schottky (low V_F)	45	10	Leaded	Diodes
SL42 to SL4	Schottky (low V_F)	20-30	4	SMD	Vishay
SBR1045SP5	Schottky (low V_F)	45	10	SMD	Diodes

Table 9. List of Recommended Diodes That May be used with LinkSwitch-3 Designs.

As the output voltage is sampled at the switching frequency, a minimum switching frequency is maintained at no-load to give acceptable transient load performance. With this minimum switching frequency and minimum drain current limit, the LinkSwitch-3 will always process a minimum amount of power to the output of the power supply, this minimum power processed is equal to

$$1/2 \times L_P \times (I_{PK}^2) \times f_{MIN}$$

Where L_P is the primary inductance; I_{PKMIN} is the minimum current limit; f_{MIN} is the minimum switching frequency.

This minimum amount of energy has to be dissipated in the pre-load resistor, clamping circuits and bias winding circuits. If the total energy dissipation in the pre-load resistor, clamping circuits and bias winding circuits is less than the calculated minimum energy, the output voltage will increase to balance the excess of energy transferred to the output. Therefore, the proper selection of the pre-load resistor is needed to prevent the output voltage from rising under very light load or no-load condition.

For designs where output voltage regulation must be maintained at zero load, start with a resistor value that represents a load of approximately 25 mW at the nominal output voltage. For example, for a 5 V output use a pre-load resistor value of 1 kΩ. For designs where the output voltage can rise under no-load conditions, select the pre-load resistor value such that the output voltage is within the maximum output voltage specification. Limit the maximum voltage rise at no-load to <50% of the normal output voltage to minimize increases in input power due to increases in the primary clamp and bias winding dissipation.

Since a pre-load resistor also increases the no-load losses, where the specification allows, adjust the no-load voltage to trade-off lower no-load input power with high no-load output voltage as needed.

Step 9 – Select Output Capacitor and Optional Post Filter

Select the capacitor voltage to be ≥1.2 × $V_{O(MAX)}$.
Select the initial capacitor choice using the maximum allowable equivalent series resistance (ESR) expression below:

$$ESR_{MAX} = \frac{V_{RIPPLE(MAX)}}{I_{SP}}$$

Where $V_{RIPPLE(MAX)}$ is the maximum specified output ripple and noise and I_{SP} is the secondary peak current from the Transformer Secondary Parameters section of the design spreadsheet.

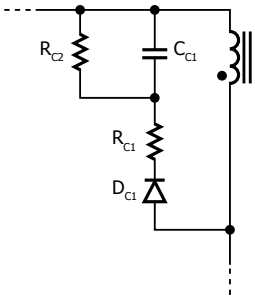
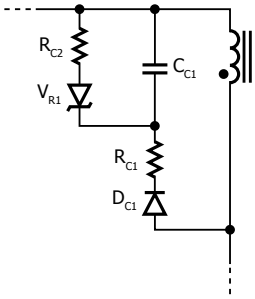
Common Primary Clamp Configurations	
RCD	**RCDZ (Zener Bleed)**
 PI-5107-042715	 PI-7330-042715
D_{C1}: 1N4007 / FR107, 1 A, 1000 V R_{C1}: 100 Ω - 300 Ω, 1/4 W C_{C1}: 470 pF - 1000 pF R_{C2}: 330 kΩ - 680 kΩ, 1/2 W	D_{C1}: 1N4007 / FR107, 1 A, 1000 V V_{R1}: BZY97Cxxx (xxx = 1.1 to 1.2 × V_{OR}) R_{C1}: 100 Ω - 300 Ω, 1/4 W R_{C2}: 5 kΩ - 100 kΩ, 1/2 W C_{C1}: 470 pF - 1000 pF

Figure 18. Primary Clamp Configurations Suitable for LinkSwitch-3 Designs.

The absolute minimum capacitance (excluding the effect of ESR) is given by:

$$C_{OUT(MIN)} = \frac{I_{O(MAX)}\left(\frac{1}{F_S} - D_{CON}\right)}{V_{RIPPLE(MAX)}}$$

Where $I_{O(MAX)}$ is the maximum output current, F_S is switching frequency, D_{CON} is the output diode conduction time and $V_{RIPPLE(MAX)}$ is the maximum allowable output ripple voltage. Verify that the ripple current rating of the capacitor is ≥ the I_{RIPPLE} value (from the Transformer Secondary Parameters section of the design spreadsheet). If not, select the smallest capacitance value that meets this requirement. Many capacitor manufacturers provide factors that increase the ripple current rating as the capacitor operating temperature is reduced from the data sheet maximum. This should be considered to ensure that the capacitor is not oversized for cost reasons.

To reduce the physical size of the output capacitor an output LC post filter can be used to reduce the ESR related switching noise. In this case, select either a 1 μH to 3.3 μH inductor with a current rating ≥I_O or a ferrite bead for designs with I_O <~500 mA. The second capacitor is typically 100 μF or 220 μF with a low ESR for good transient response. As the secondary ripple current does not pass through this capacitor there are no specific ESR or ripple current requirements.

Step 10 – Selection of Primary Clamp Components

Two clamp arrangements, shown in Figure 18, are suitable for LinkSwitch-3 designs. Minimize the value of C_{C1} and maximize R_{C2} while maintaining the peak drain voltage to <680 V. Larger values of C_{C1} may cause higher output ripple voltages due to the longer settling time of the clamp voltage impacting the sampled voltage on the feedback winding.

A value of 200 kΩ with 470 pF capacitor is a recommended starting point for the RCD design. Verify that the peak drain voltage is less than 680 V under all line an load conditions.

The RCDZ circuit is preferred when the primary leakage inductance is greater than 125 μH to reduce drain voltage overshoot and/or ringing present on the feedback winding.

For best output regulation, the feedback voltage must settle to within 1% at 2.1 μs from the turn-off of the primary MOSFET.

This requires careful selection of the clamp circuit components. The voltage of V_{R1} is selected to be 10% to 20% above the V_{OR}. This allows the clamp to limit the magnitude of the leakage voltage spike at turn-off but ensures the Zener is not conducting during the flyback period when the output diode is conducting. The value of R_{C2} should be the largest value that result in both acceptable settling of the FEEDBACK pin voltage and peak drain voltage. Making R_{C2} too large will increase the discharge time of C_{C1}, increase the peak drain voltage and degrade regulation.

Resistor R_{C1} dampens high frequency leakage inductance ringing for reduced EMI. The value must be large enough to dampen the ring in the required time but must not be too large to cause the drain voltage to exceed 680 V.

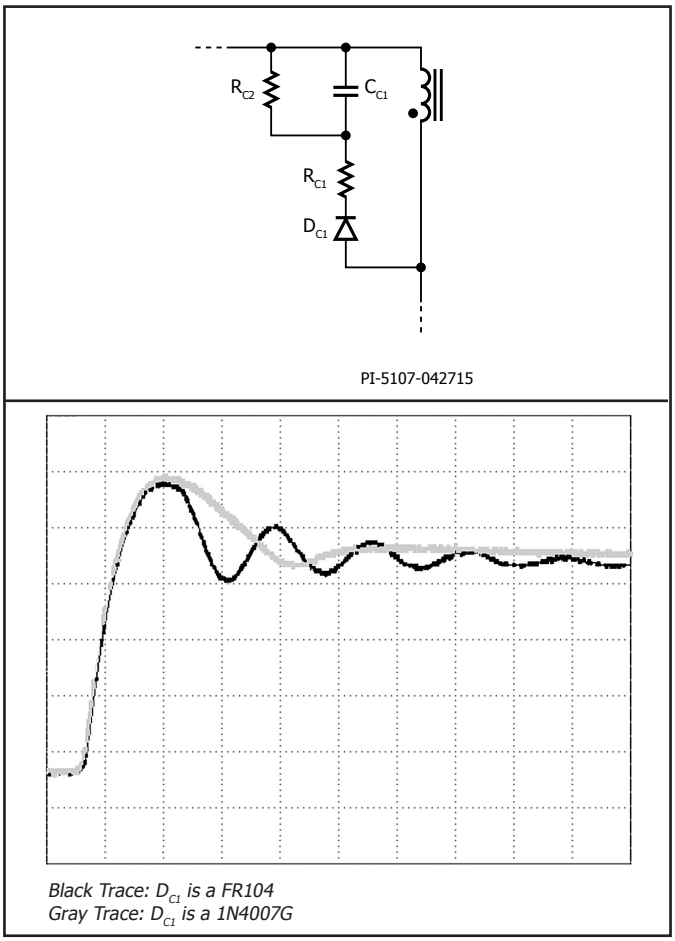


Figure 19. Effect of Clamp Diode Recovery Time of FEEDBACK Pin Voltage.

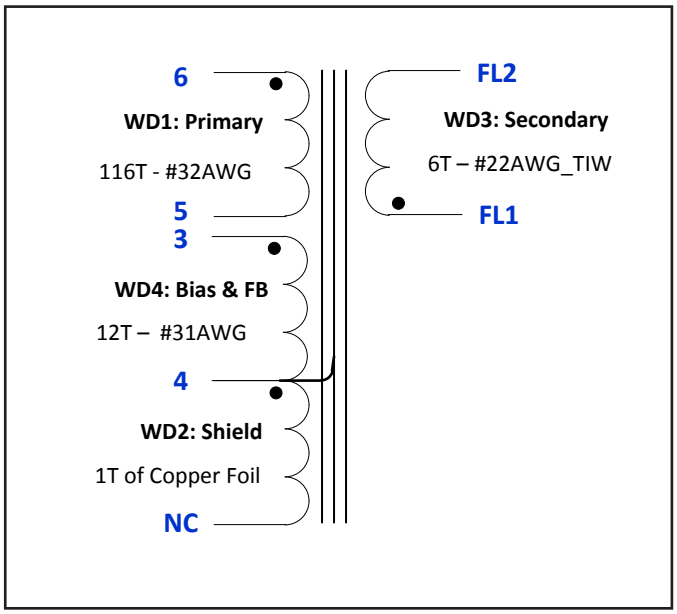


Figure 20. Typical Transformer with Copper Foil Shield.

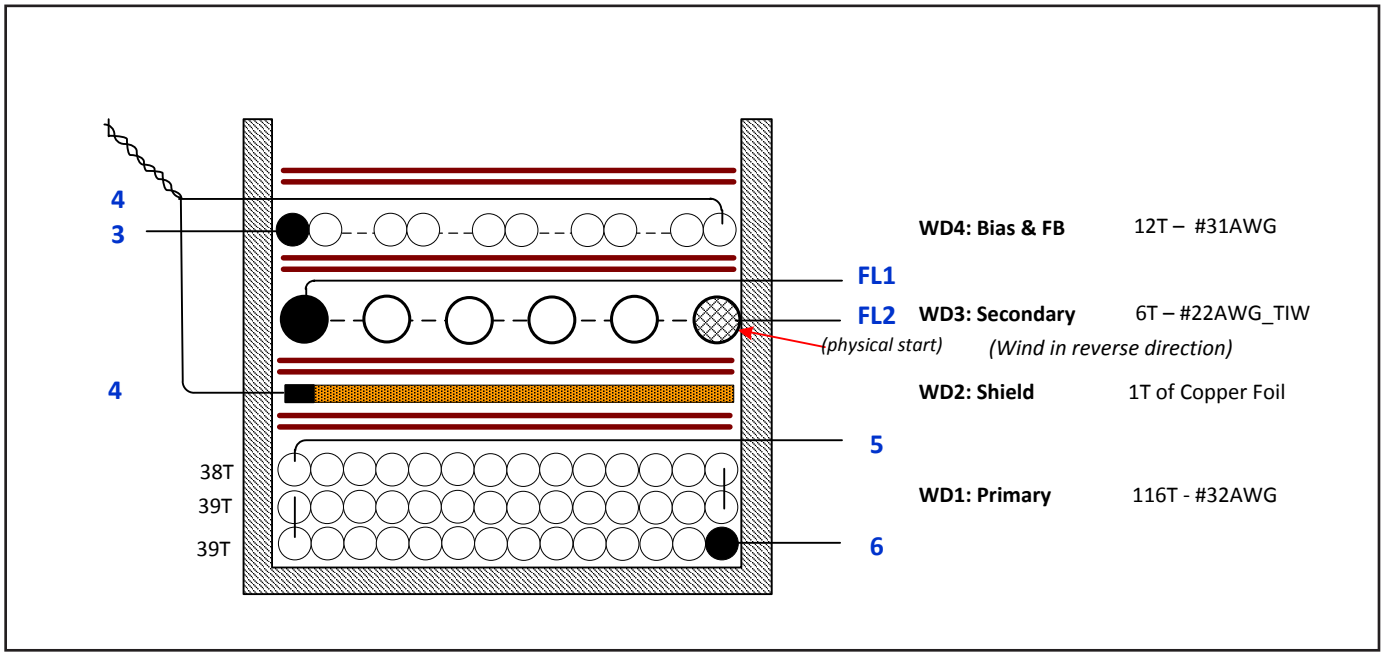


Figure 21. Typical Mechanical Construction of LinkSwitch-3 Transformer with Copper Foil Shield.

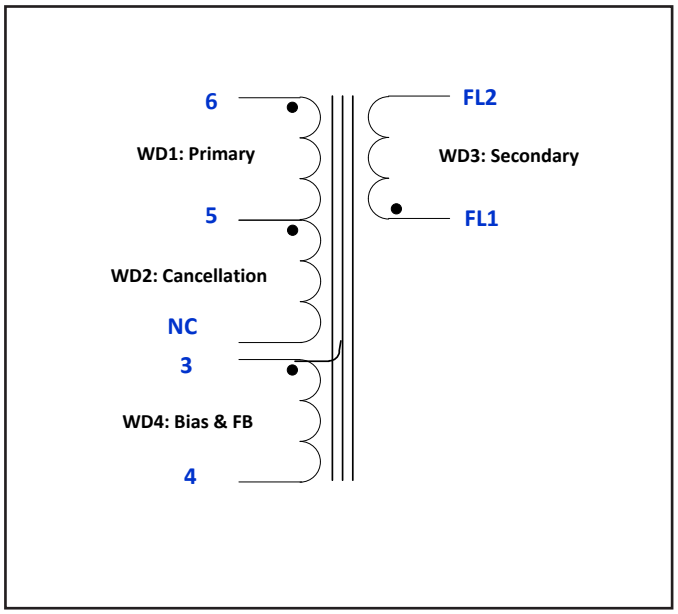


Figure 22. Typical Transformer with Shield Winding.

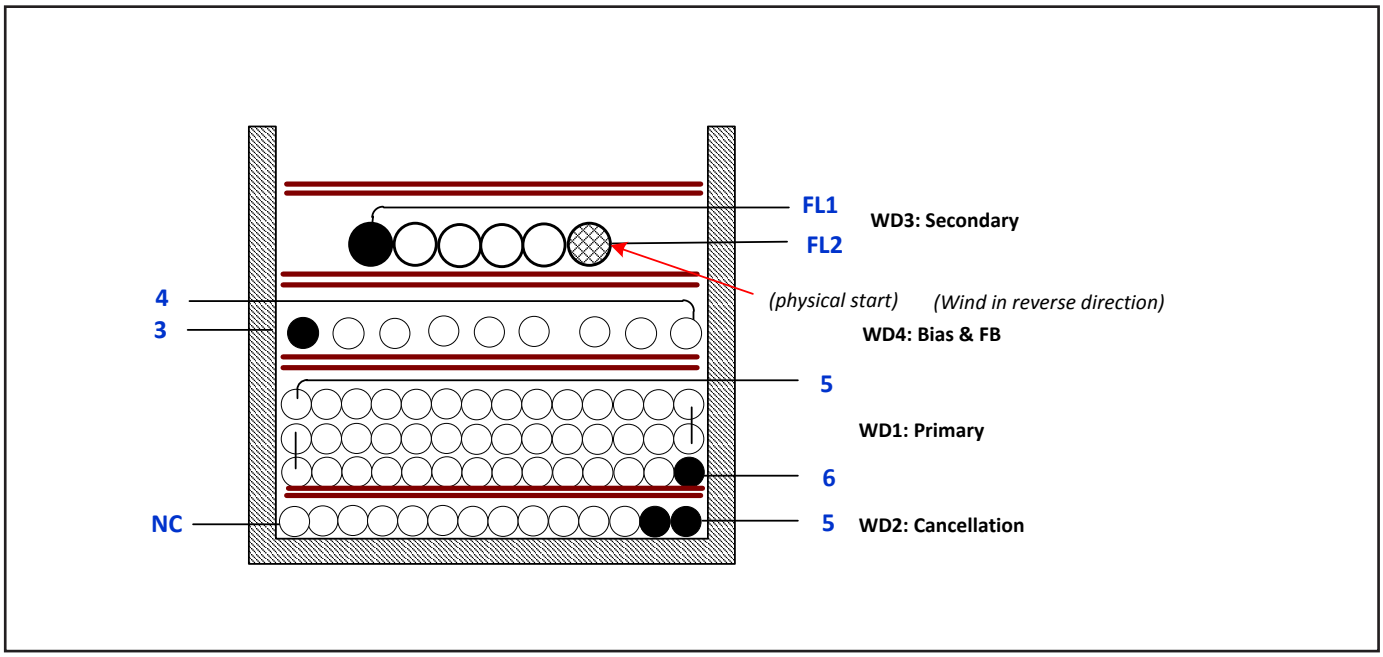


Figure 23. Typical Mechanical Construction of LinkSwitch-3 Transformer with Shield Winding.

If the primary leakage inductance is less than 125 μH, V_{R1} can be eliminated and the value of R_{C2} increased. A value of 470 kΩ with an 820 pF capacitor is a recommended starting point. Verify that the peak drain voltage is less than 680 V under all line and load conditions. Verify the feedback winding settles to an acceptable limit for good line and load regulation.

Effects of Fast vs. Slow Diodes in Clamp Circuit

A slow reverse recovery diode (>1 μs) reduces the feedback voltage ringing and improve output regulation. Using a fast diode (500 ns) increases the amplitude of ringing which can result in increased output ripple. In Figure 19 the (larger) ring amplitude when using a FR104 diode represents up to an 8% error in the sampled voltage over the time period 2.5 μs to 3.1 μs.

Example Transformer Winding Arrangement Including E-Shields™

Once the PIXls spreadsheet design is complete all the necessary information is available to create a transformer design. In this section some practical tips are presented on winding order and the inclusion of Power Integrations proprietary E-Shield techniques. Shield windings improve conducted EMI performance and simplify the input

filter stage by eliminating the need for a common mode choke and reducing the value of or eliminating the Y-class capacitor connected between the primary and secondary. Refer to Figures 20, 21, 22 and 23 to reference winding numbers (WDx).

Copper Foil Shield
A copper foil shield (WD2) included in the transformer design of Figure 21 between the primary winding to the secondary winding, this shield copper foil prevents the noise from the primary-side and reduce the conductive emission level of the power supply. Transformer with copper foil shield shows very consistent EMI performance.

Shield Winding
A less expensive method of shielding is to use E-Shield techniques. In Figure 23, the first layer of the transformer is a cancellation shield winding (WD2). Calculate the number of turns by taking the number of primary turns N_P [D74] from PIXls and dividing it by the number of layers L [D56]. Divide the result by 2 ($N_{SHEILD} = 0.5 \times (N_P/L)$). This gives a starting value which may need to be adjusted to minimize conducted EMI emissions. The finish end of the shield winding is floating. Select a wire gauge that completely fills the bobbin width.

Primary Winding
The second winding (WD1) is the primary. From PIXls find the number of turns N_P [D74], number of layers L [D56] and the wire gauge AWG [D86]. As shown in Figure 23, the start of the primary is the drain node of the MOSFET. An optional 1 mm tape can be used to improve EMI repeatability by making the transformer design less sensitive to production variation. To include the tape margin, enter a margin value of 1 mm into cell [B55] of the PIXls spreadsheet.

Feedback Winding and Bias Winding
From PIXls find the number of turns N_{FB} [D30]. To reduce conducted EMI emissions, this winding must cover the complete bobbin width. A multi-filar winding is used to achieve this and some experimentation may be needed to find the optimum wire gauge and number of filar (parallel winding wires). Generally more than 4 filar is not recommended due to manufacturability considerations when multi-filar windings are terminated onto a single bobbin pin.

Secondary Winding
From PIXls find the number of secondary turns NS [D57]. Start the secondary winding on the same side of the bobbin as the start of the feedback winding. Select a gauge wire to completely fill the bobbin winding window width. Triple-insulated wire is recommended for the secondary winding to avoid the need to use wide tape margins to meet safety spacing requirements (6 mm to 6.2 mm typical) and minimize the transformer core size required.

Tips for Designs

Reflected Output Voltage (V_{OR}) Adjustment
Users of design spreadsheets for other Power Integrations device families may notice that some parameters (V_{OR}, N_S and N_P) cannot be changed directly in the LinkSwitch-3 spread-sheet. To change these parameters, use the relationships shown below:

V_{OR}: Increasing D_{CON} or F_S will decrease the value of V_{OR}
N_S: Increasing D_{CON} decreases N_S
N_P: Determined by $B_{M(TARGET)}$

CV Regulation
The tight tolerances of the FEEDBACK Pin Voltage (V_{FBth}) and small temperature coefficient (TC_{VFB}) provide tight regulation of the output voltage during CV operation.

There are two main factors that have to be addressed to optimize the output voltage difference at zero and full load:

1. No-load voltage rise.
2. Cable drop compensation.

For the no-load voltage rise, there are several factors related to this output voltage rise: Pre-load resistor selection, which is covered in Step 8 (Selection of Output Diode and Pre-Load); resistor R4 (Figure 16) in the bias winding, too low R4 value may cause higher output voltage rise at no-load; transformer designed at lower switching frequency with higher primary inductance, which ends up with higher no-load energy delivers to the main output.

For the cable drop compensation, LinkSwitch-3 provides cable drop compensation options; the amount of cable drop compensation is determined by the third digit in the device part number. The required compensation is based on the cable resistance that includes the connector resistance, not only the cable. For example, if the cable resistance is 150 MΩ, the voltage drop at full load (5 V and 2 A for example) is 0.15 Ω × 2 A = 0.3 V, then the 6% cable compensation part should be selected to compensate 5 V × 6% = 0.3 V voltage drop. Figure 24 shows the output voltage in the end of the cable with different cable drop compensation performance, cable drop compensation has to be optimized if it is over compensated or under compensated.

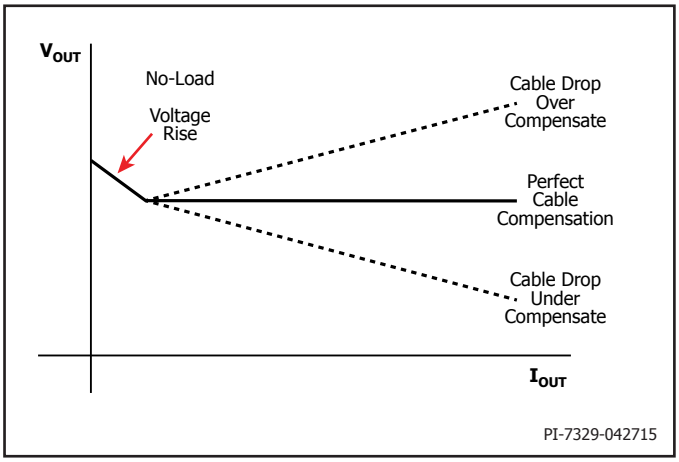


Figure 24. CV Regulation Output Voltage in the End of the Cable.

CV and CC Level Centralization
LinkSwitch-3 provides an overall output tolerance (including line, component variation, and temperature) of ±5% for the output voltage in CV operation and ±10% for the output current during CC operation, over a junction temperature range of 0 °C to 110 °C.

The way to adjust the CV regulation level and keep the CC level constant is to adjust the ratio of the FEEDBACK pin resistor R_{UPPER}/R_{LOWER}, and proportionally increase and decrease the output power. Figure 25 shows the CV regulation moves with the changing of the ratio of R_{UPPER}/R_{LOWER}. The way to adjust the CC level is to keep the ratio of R_{UPPER}/R_{LOWER} to be constant and by increasing or decreasing the R_{UPPER} and R_{LOWER} at the same time. The CV regulation is unaffected, while the CC level is decreased or increased. Figure 26 shows the CC level moves with keeping the ratio R_{UPPER}/R_{LOWER} constant and increasing and decreasing the R_{UPPER} and R_{LOWER} at the same time. It is advised to test at least 30 pcs of boards to choose the optimized FEEDBACK pin resistor for CV regulation and CC level.

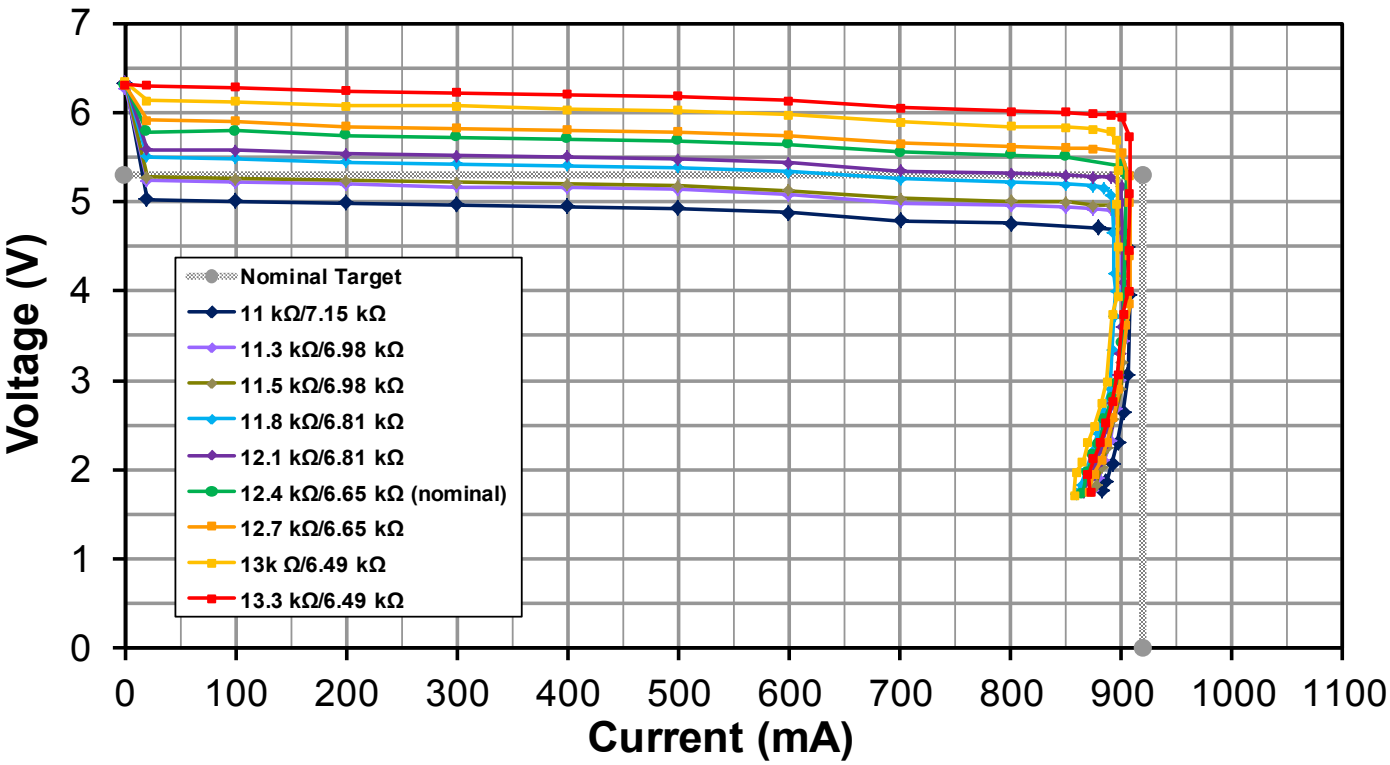


Figure 25. Example of CC/CV Centralization by Adjusting the Ratio R_{UPPER}/R_{LOWER}, Proportionally Increasing/Decreasing the Output Power to Keep CC Constant.

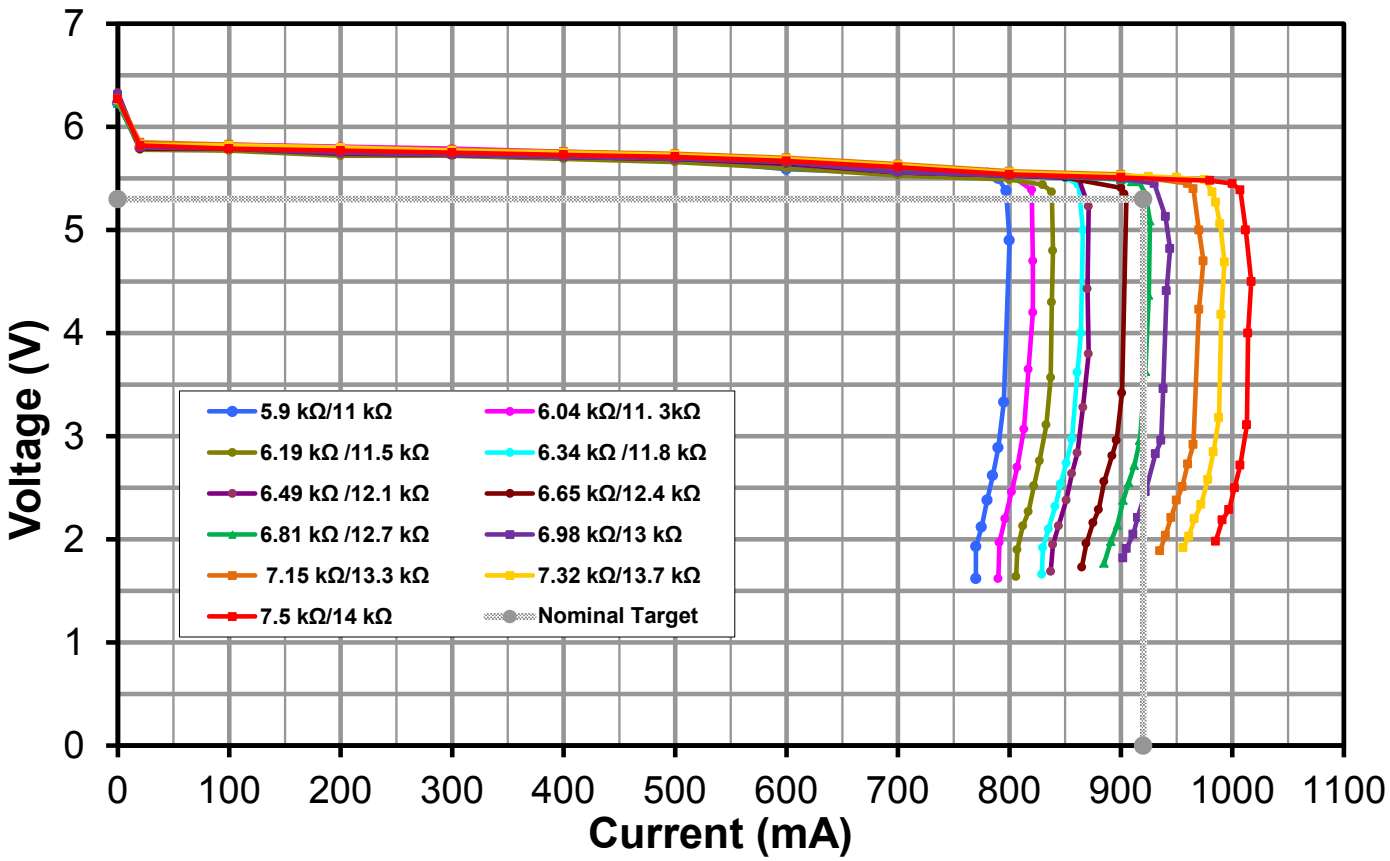


Figure 26. Example of CC/CV Centralization by Adjusting the FEEDBACK Pin Resistor (R_{UPPER} and R_{LOWER}), Keep Ratio R_{UPPER}/R_{LOWER} Constant.

Transient Load Response

LinkSwitch-3 is a primary-side control IC. The feedback is generated by the transformer bias winding every time that a single pulse is delivered. The IC has no information about the output status between the two consecutive pulses. The worst-case reaction time for the power supply is $1/F_{SW(MIN)}$, so the transient response is a function of the minimum operation switching frequency. As what Figure 27 shows, the minimum transient voltage is composed by region 1 and region 2.

The voltage drop in region 1 is caused by the voltage drop through the cable resistor.

$$\Delta V_1 = I_{OUT} \times R_{CABLE}$$

Where R_{CABLE} is the cable resistance.

The voltage drop in region 2 is caused by the voltage drop through the cable resistor.

$$\Delta V_2 = I_{OUT} \times (t_2 - t_1)/C_{OUT}$$

Where C_{OUT} is the output capacitor value, $1/(t_2-t_1)$ is the minimum switching frequency. The voltage drop in region 2 is function of the output capacitor and the switching frequency. Increasing the output capacitor will improve the undershoot voltage during the transient load, and increasing the minimum switching frequency by decreasing the pre-load resistor can help to improve the understood voltage as well. Decreasing the pre-load resistor which causes higher no-load consumption should be noted.

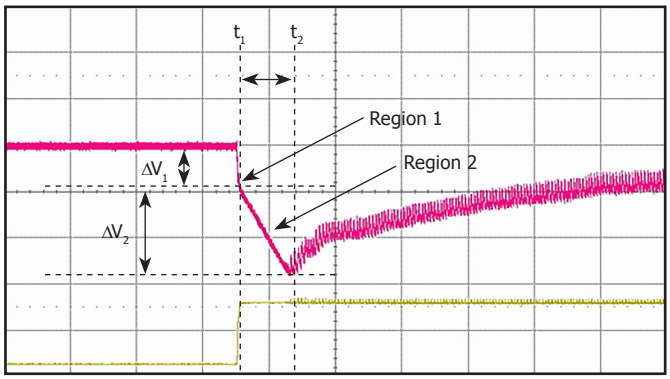


Figure 27. Output Voltage at the end of the Cable and Load Current.

Design Recommendations

Circuit Board Layout

LinkSwitch-3 is a highly integrated power supply solution that integrates on a single die both the controller and the high-voltage MOSFET. The presence of high switching currents and voltages together with analog signals makes it especially important to follow good PCB design practices to ensure stable and trouble-free power supply operation. See Figures 28 and 29 for recommended circuit board layouts for the LinkSwitch-3. When designing a printed circuit board for the LinkSwitch-3 based power supply, it is important to follow the guidelines that follow. Figure 30 shows an improper layout design example.

Single-Point Grounding

Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the LinkSwitch-3 SOURCE pin and bias winding return. This improves surge capabilities by returning surge currents from the bias winding directly to the input filter capacitor.

Bypass Capacitor

The BYPASS pin capacitor should be located as close as possible to the SOURCE and BYPASS pins.

Feedback Resistors

Place the feedback resistors directly at the FEEDBACK pin of the LinkSwitch-3 device. This minimizes noise coupling.

Thermal Considerations

The copper area connected to the SOURCE pins provides the LinkSwitch-3 heat sink. A good estimate is that the LinkSwitch-3 will dissipate 10% of the output power. Provide enough copper area to keep the SOURCE pin temperature below 110 °C. Higher temperatures are allowable only if an output current (CC) tolerance above ±10% is acceptable in your design. In this case, a maximum SOURCE pin temperature below 110 °C is recommended to provide margin for part-to-part $R_{DS(ON)}$ variation. A small copper area for heat sinking should always be avoided.

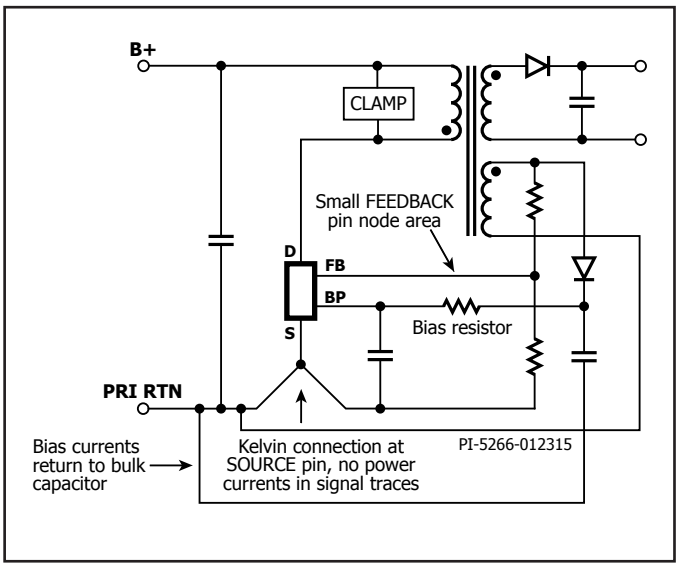


Figure 28. Schematic Representation of Recommended Layout.

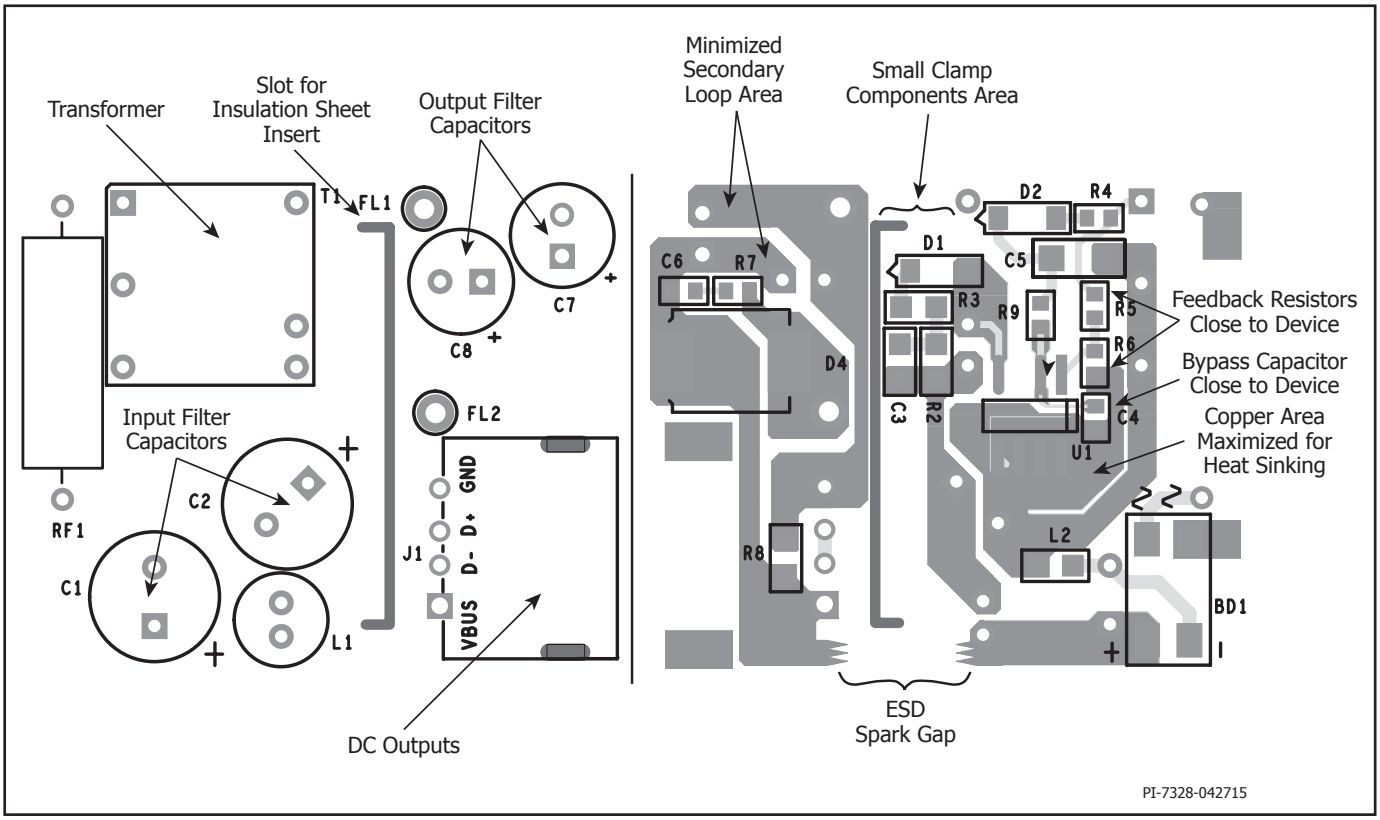


Figure 29. PCB (Top Left) (Bottom Right) Layout Example Showing 10 W Design using P Package.

Secondary Loop Area
To minimize reflected trace inductance and EMI minimize the area of the loop connecting the secondary winding, the output diode, and the output filter capacitor. In addition, provide sufficient copper area at the anode and cathode terminal of the diode for heat sinking. Provide a larger area at the quiet cathode terminal. A large anode area can increase high frequency radiated EMI.

Electrostatic Discharge Spark Gap
A trace is placed along the isolation barrier to form one electrode of a spark gap. The other electrode on the secondary is formed by the output node. The spark gap directs ESD energy from the secondary back to the AC input. The trace from the AC input to the spark gap electrode should be spaced away from other traces to prevent unwanted arcing to other nodes, and possible circuit damage.

Drain Clamp Optimization
LinkSwitch-3 senses the feedback winding on the primary-side to regulate the output. The voltage that appears on the feedback winding is a reflection of the secondary winding voltage while the internal MOSFET is off. Therefore, any leakage inductance induced ringing can affect output regulation. Optimizing the drain clamp to minimize the high frequency ringing gives the best regulation. Figure 31 shows the desired drain voltage waveform. Compare this to Figure 32 with a large undershoot, caused by ringing due to leakage inductance. This ringing, and its effects, degrades the output voltage regulation performance. To reduce this ringing (and the undershoot it may cause) adjust the value of the resistor (R3 in Figure 16) in series with the clamp diode.

Quick Design Checklist

As with any power supply design, verify your LinkSwitch-3 design on the bench to make sure that component specifications are not exceeded under worst-case conditions.

The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that peak V_{DS} does not exceed 680 V at highest input voltage and maximum output power.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage, and maximum output load, observe drain current waveforms at start-up for any signs of transformer saturation and excessive leading edge current spikes. LinkSwitch-3 has a leading edge blanking time of 170 ns to prevent premature termination of the ON-cycle.
3. Thermal check – At maximum output power, both minimum and maximum input voltage, and maximum ambient temperature, verify that temperature specifications are not exceeded for LinkSwitch-3, transformer, output diodes, and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of LinkSwitch-3, as specified in the data sheet. To assure 10% CC tolerance a maximum SOURCE pin temperature of 110 °C is recommended.

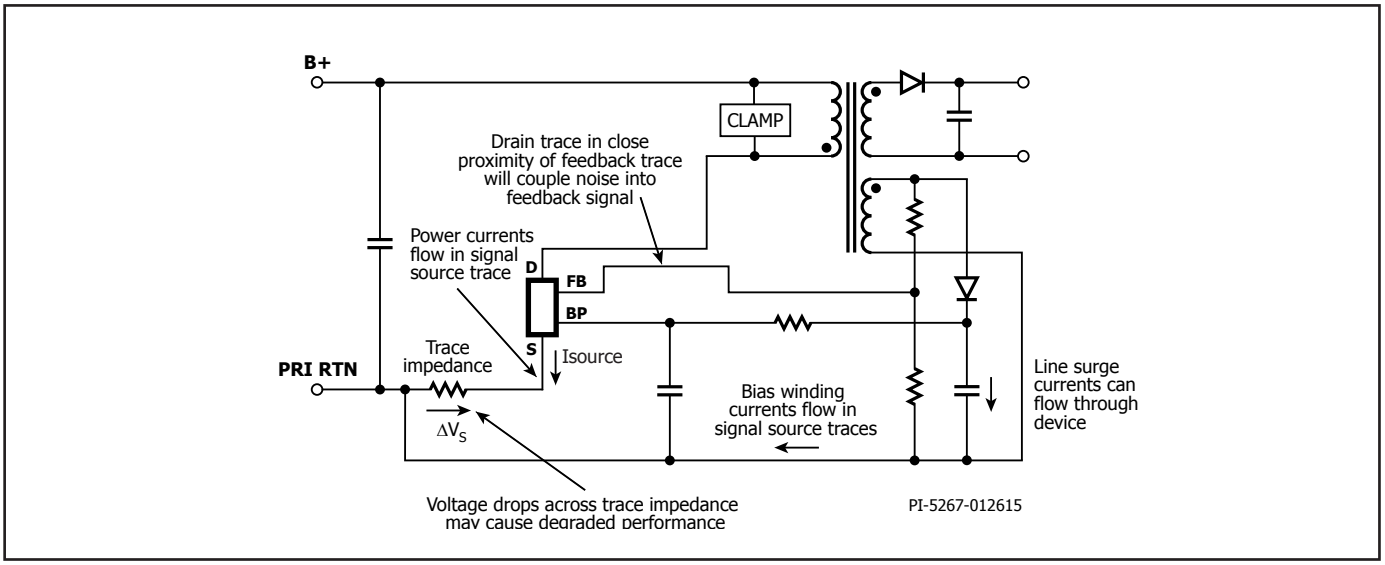


Figure 30. Schematic Representation of Electrical Impact due to Improper Layout.

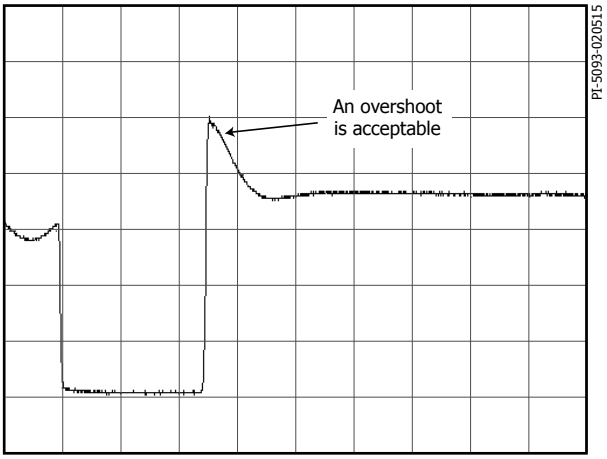


Figure 31. Desired Drain Waveform.

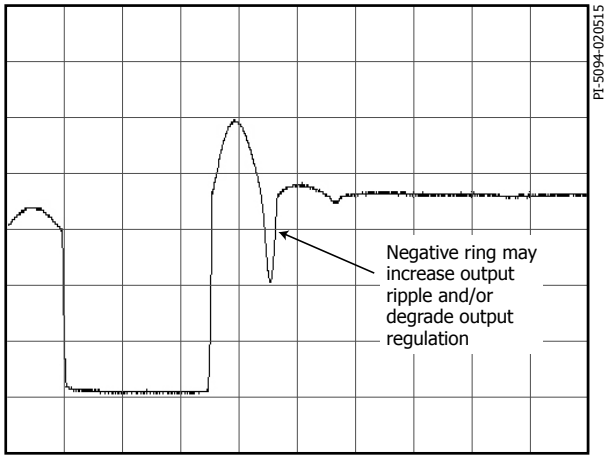


Figure 32. Undesirable Drain Waveform.

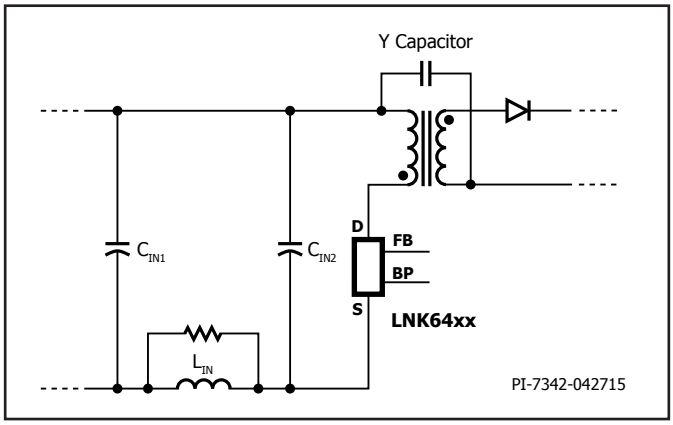


Figure 33. Correct Location of Input Inductor when using a Y Capacitor.

Notes

Revision	Notes	Date
A	Initial Release.	04/15

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