COM底板设计和开发指引

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研华嵌入式产品事业群

Agenda

- COM产品架构
  - COM-E Form Factor Design Guide
  - ETX3.0 Form Factor Design Guide

Gigabit Ethernet (GBE)

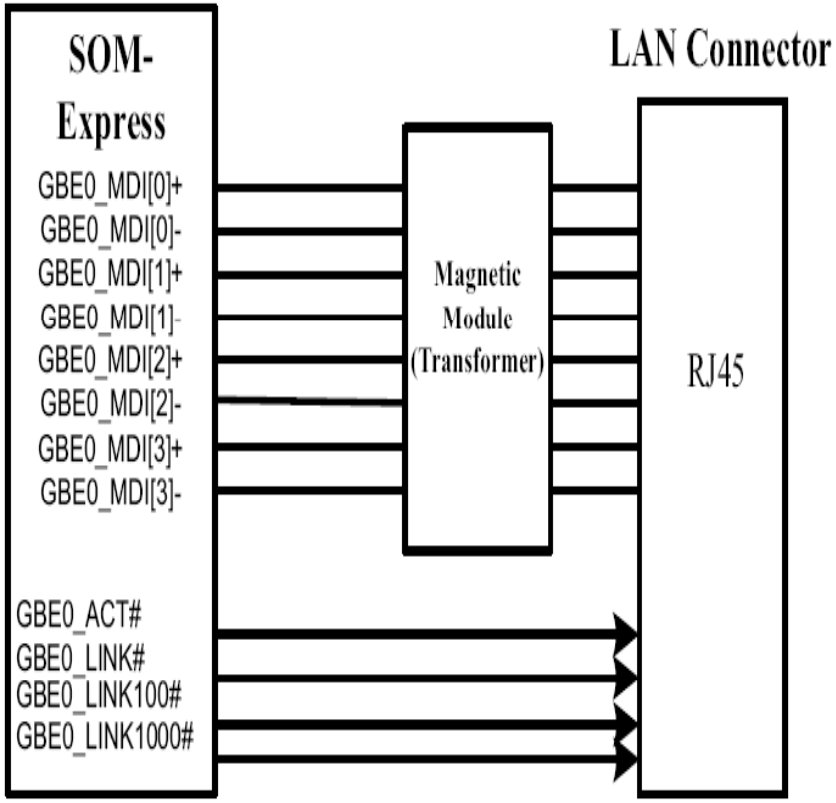
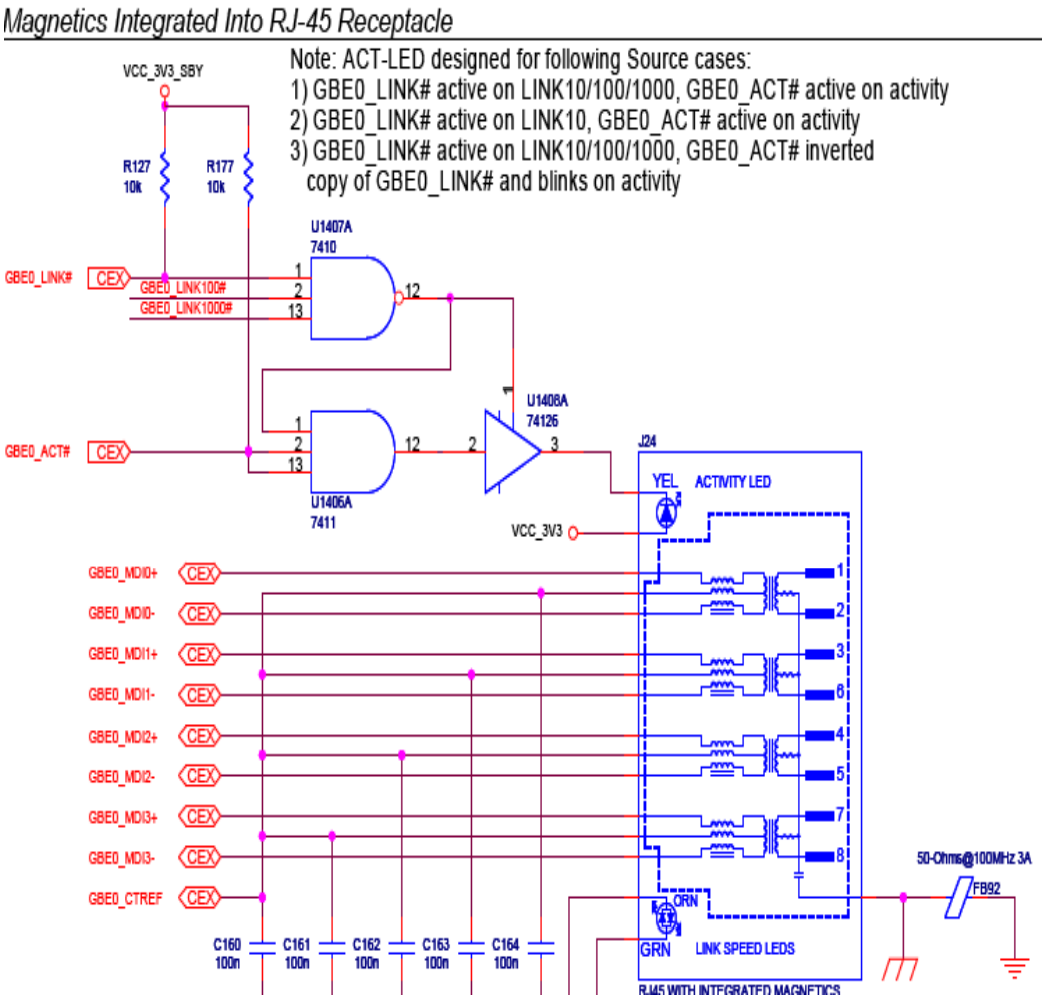


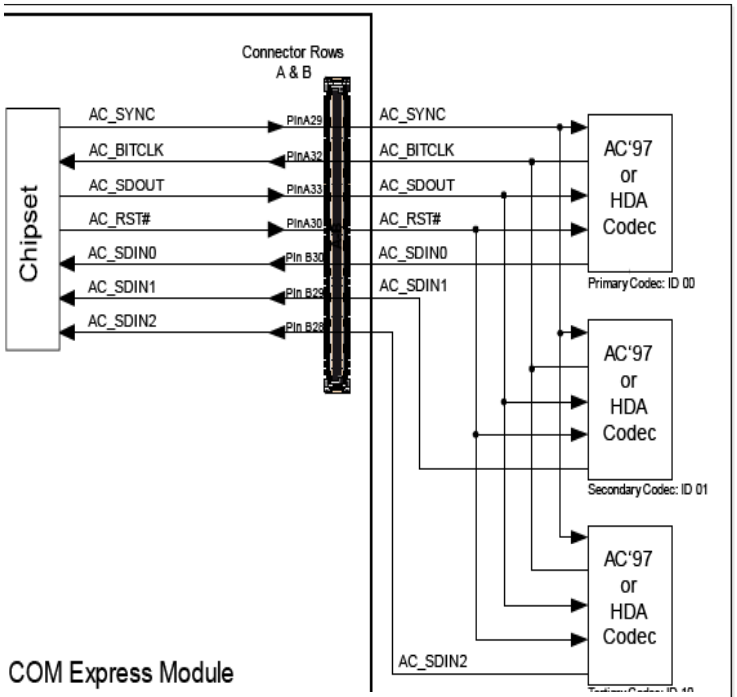
Figure 5-28 Gigabit Ethernet Connections

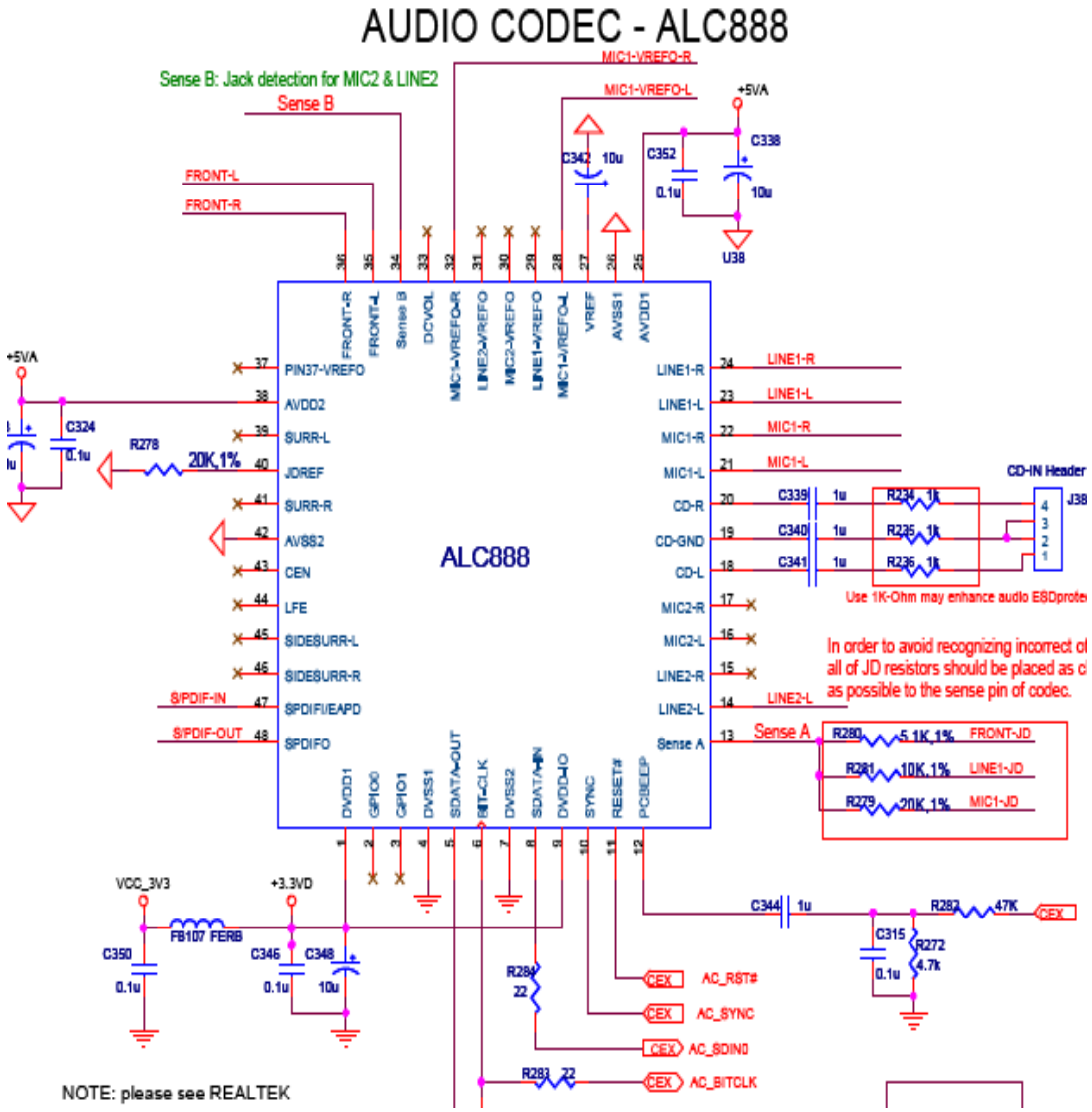


Gigabi10/100 - N/C

1000 - Connect 0Ω in series to Magnetics Module center trap and 0.1uF to ground on every pin

AC97 Audio HD Audio (AC97）

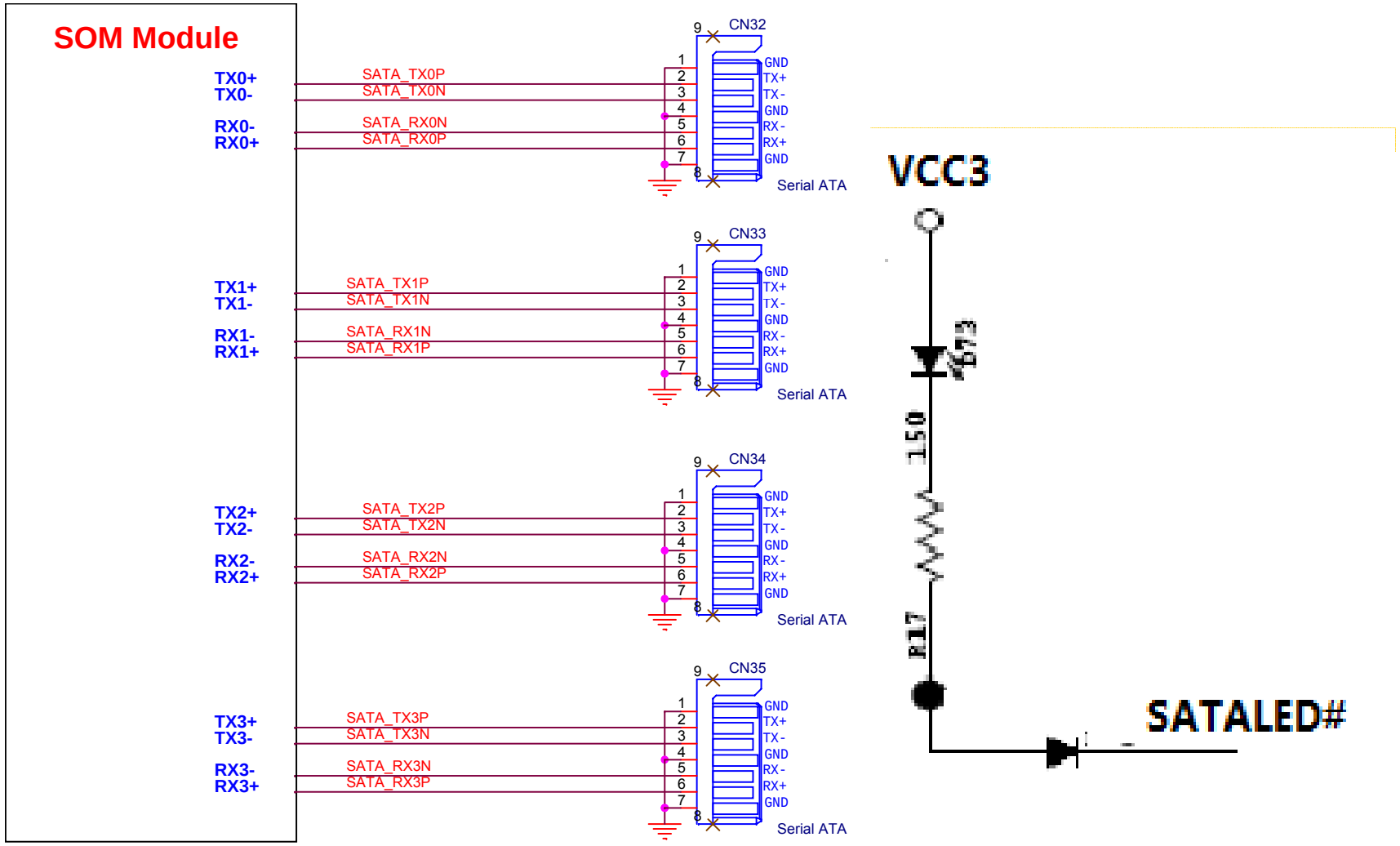




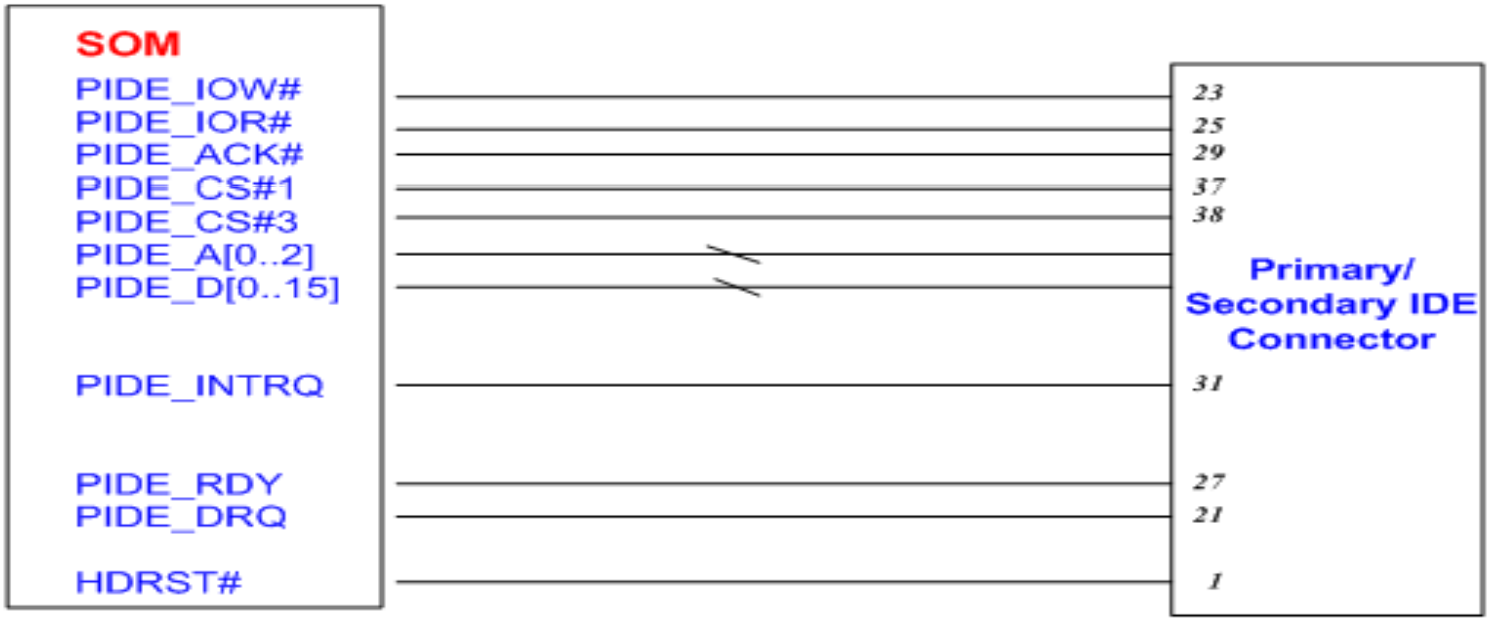
Audio Codec Signal Descriptions

Signal	Pin	Description	I/O	Comment
AC_RST#	A30	CODEC Reset.	O 3.3V Suspend CMOS	
AC_SYNC	A29	Serial Sample Rate Synchronization.	O 3.3V CMOS	
AC_BITCLK	A32	12.228 MHz Serial Bit Clock for CODEC.	O 3.3V CMOS	
AC_SDOUT	A33	Audio Serial Data Output Stream.	O 3.3V CMOS	
AC_SDIN0 AC_SDIN1 AC_SDIN2	B30 B29 B28	Audio Serial Data Input Stream from CODEC[0:2].	I 3.3V Suspend CMOS	

Serial ATA SAS (SATA)



IDE



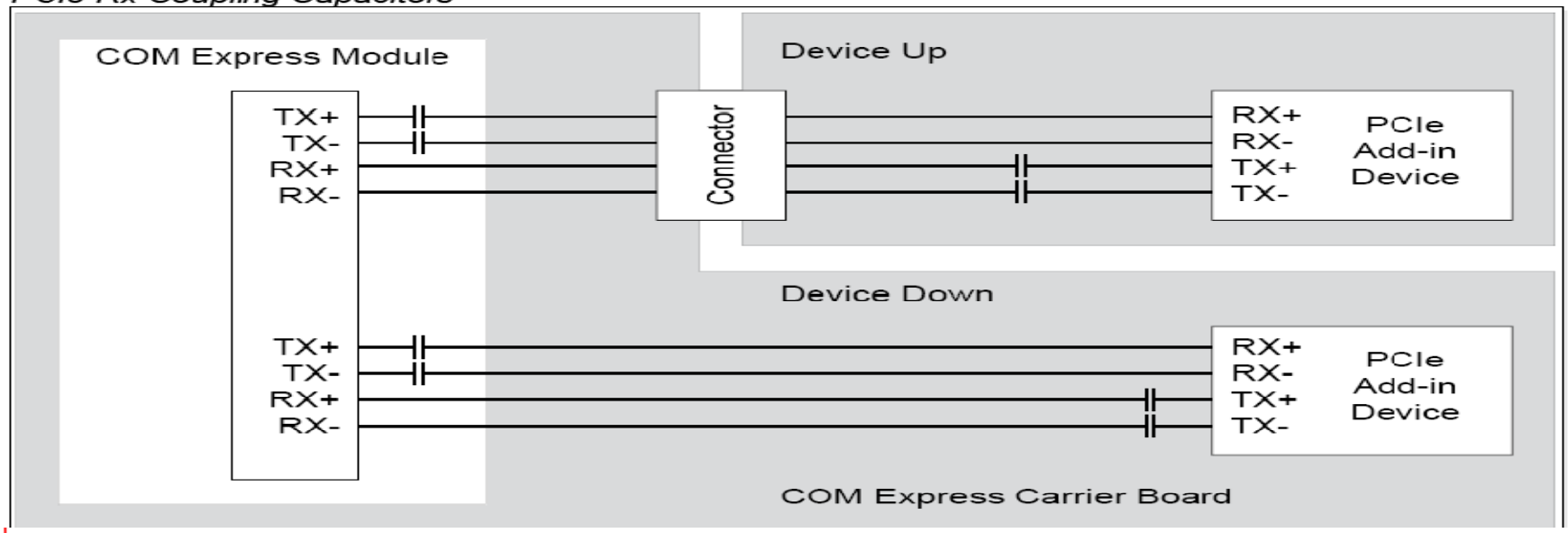
IDE Signal Groups		
Signal Group	**Primary**	**Secondary**
Data	PDD [15:0]	SDD[15:0]
Strobes	PDIOR# (write) PIORDY (read)	SDIOR# (write) SIORDY (read)

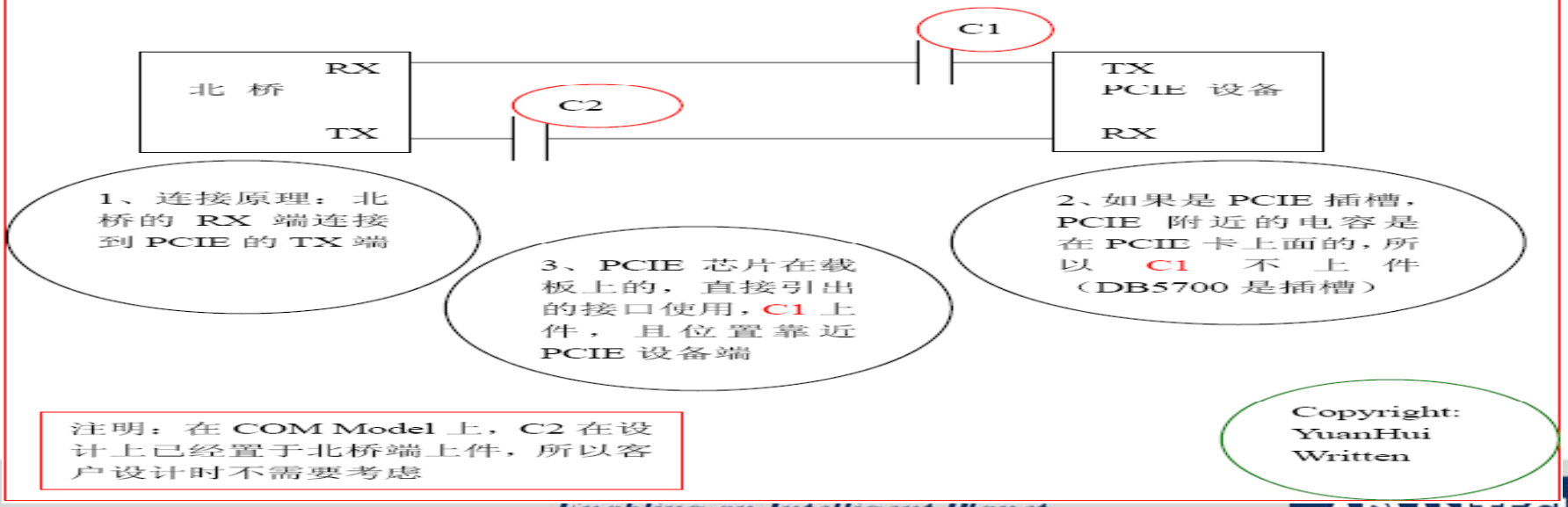
注意信号：PDIAG_S，CBLID_P

PCI Express

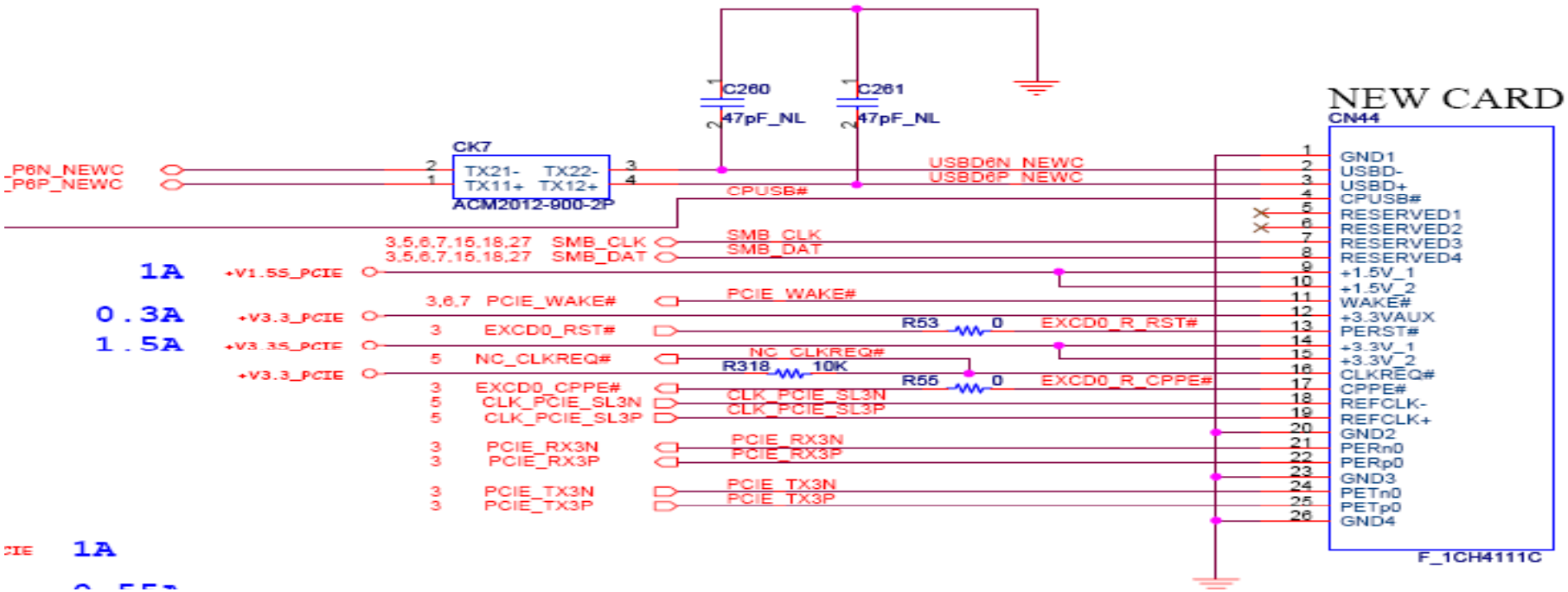
Device Up / Device Down and PCIe Rx / Tx Coupling Capacitors

PCIe Rx Coupling Capacitors

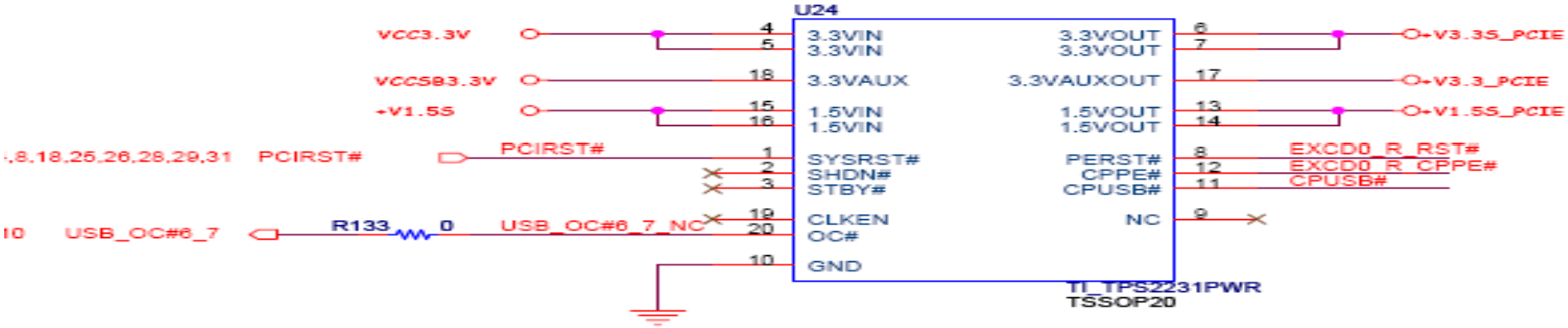




ExpressCard(EXCD)



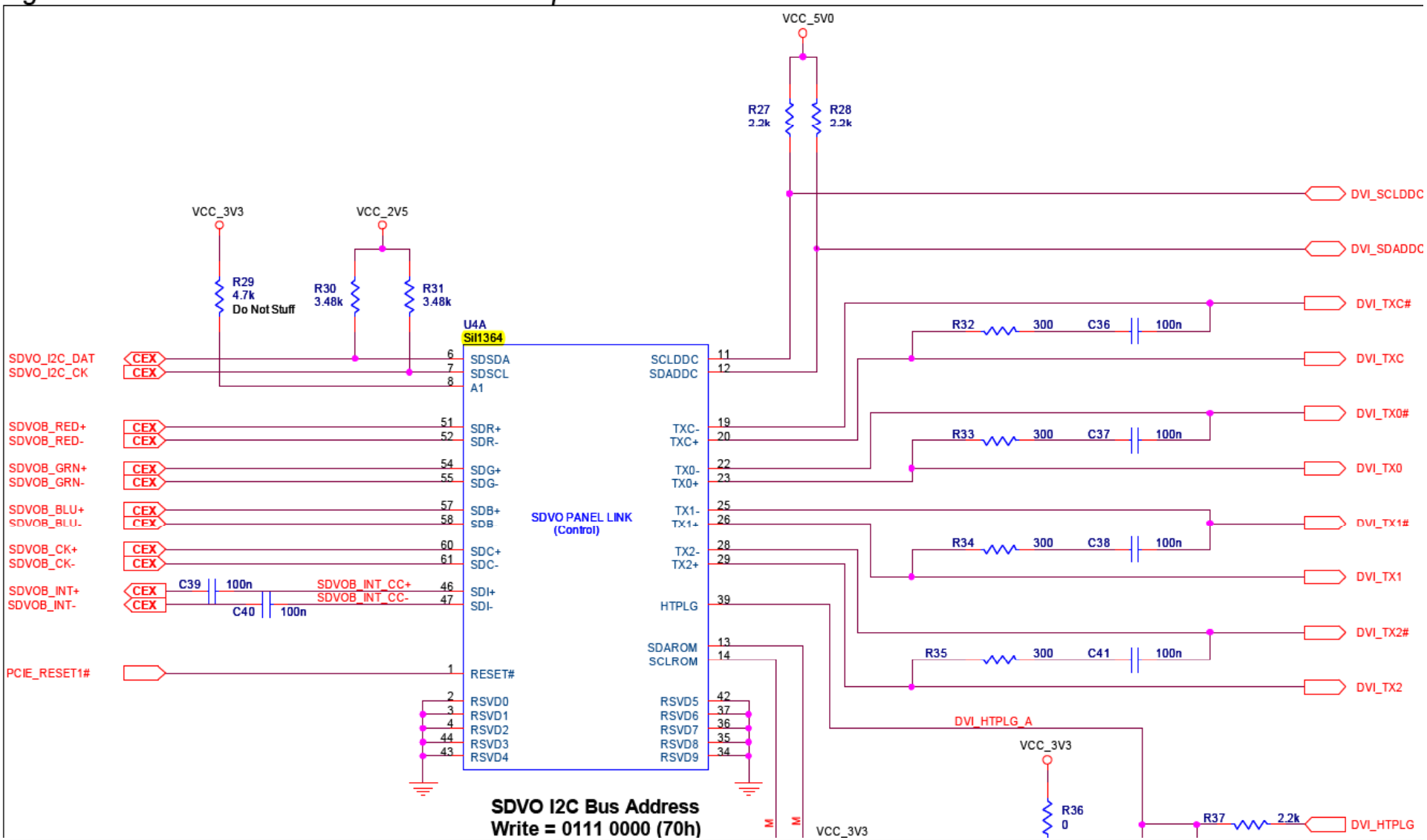
NEW CARD POWER SWITCH



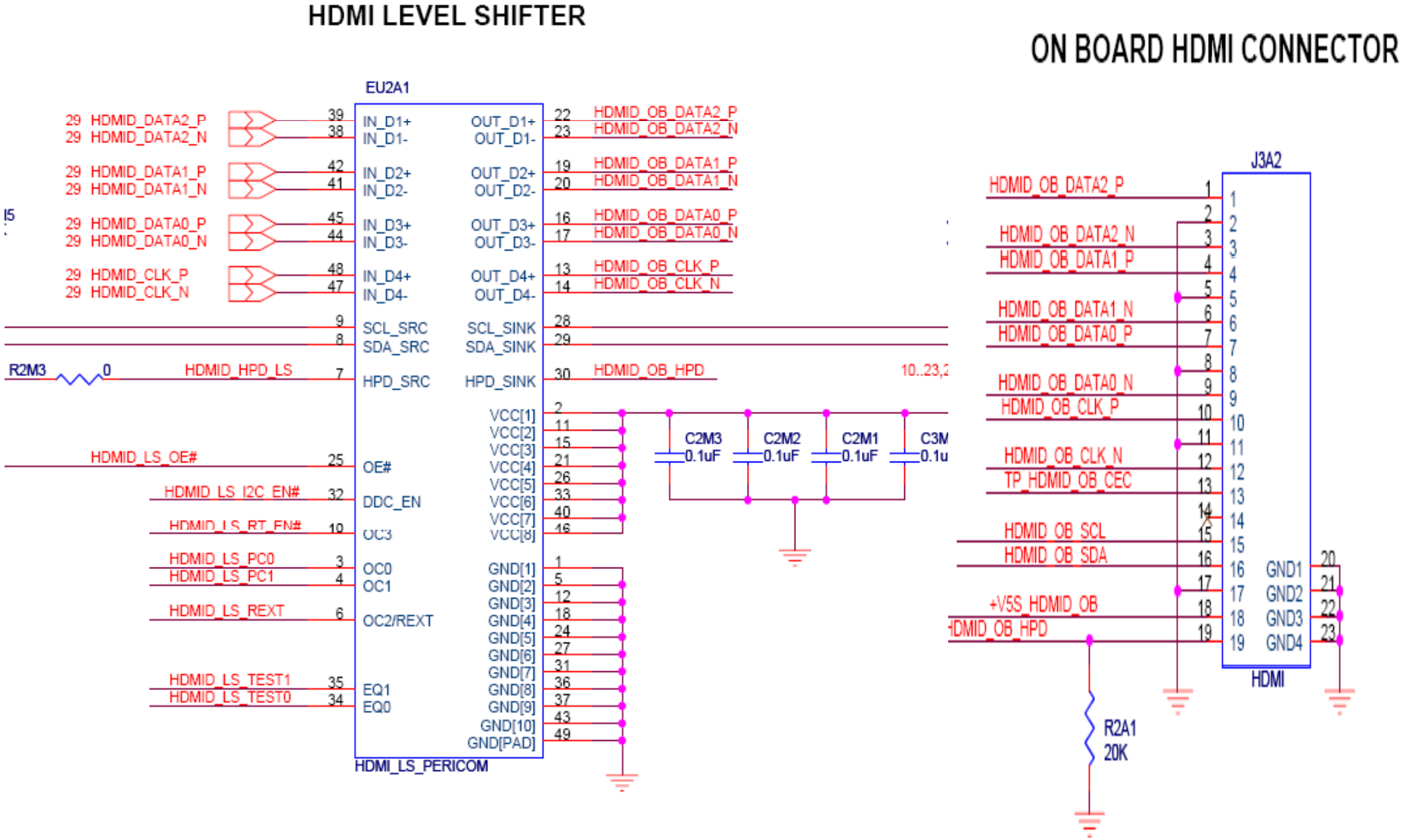
SDVO

2.5.2.1. SDVO to DVI Transmitter Example

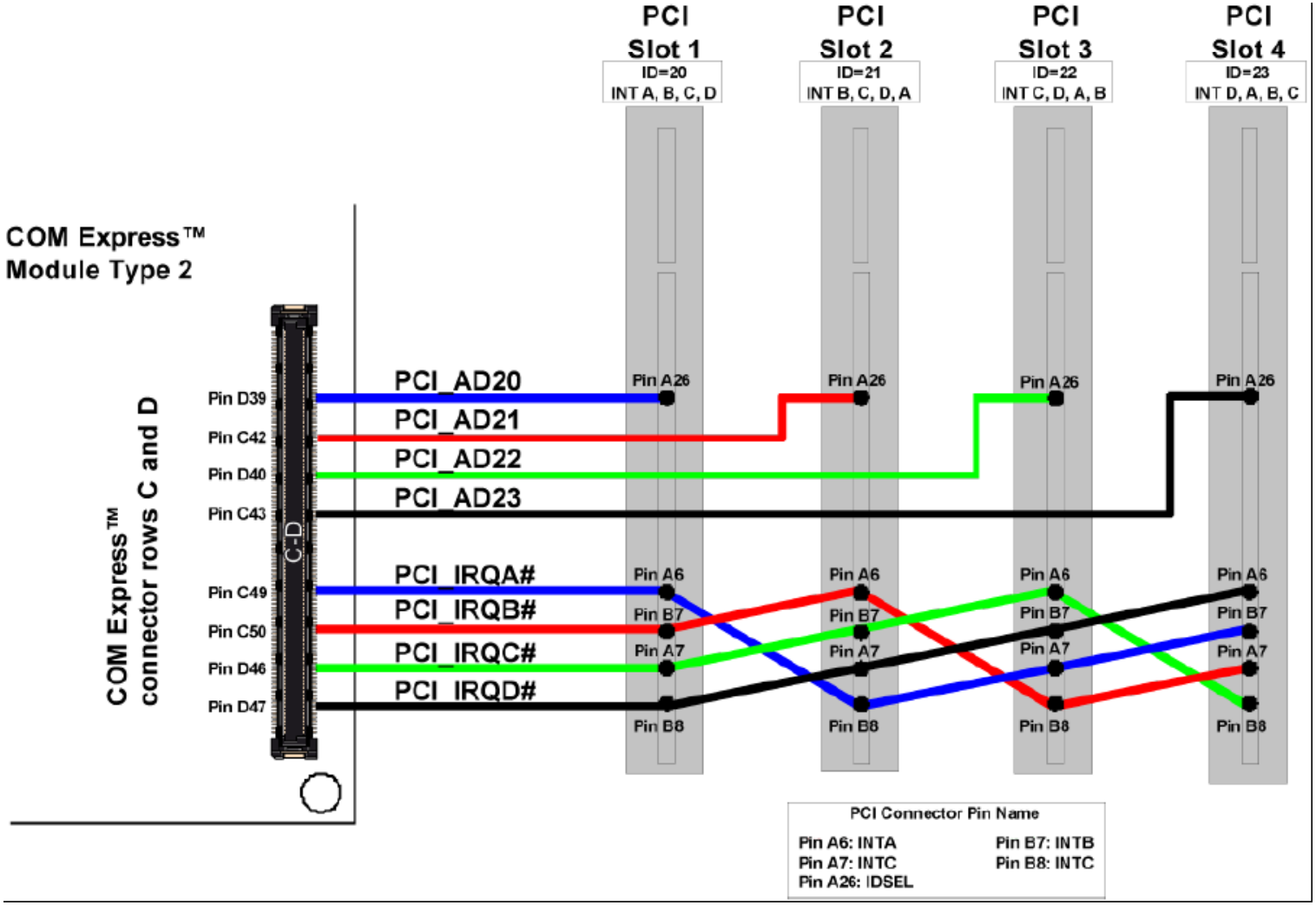
Figure 17: SDVO to DVI Transmitter Example



Display Port/DVI/HDMI



PCI


PCI Slot 1
ID=20
INT A, B, C, D
PCI Slot 2
ID=21
INT B, C, D, A
PCI Slot 3
ID=22
INT C, D, A, B
PCI Slot 4
ID=23
INT D, A, B, C
COM Express™ Module Type 2
COM Express™ connector rows C and D
C-D
Pin D39
Pin C42
Pin D40
Pin C43
Pin C49
Pin C50
Pin D46
Pin D47
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
PCI_IRQA#
PCI_IRQB#
PCI_IRQC#
PCI_IRQD#
Pin A26
Pin A6
Pin B7
Pin A7
Pin B8
PCI Connector Pin Name
Pin A6: INTA
Pin A7: INTC
Pin A26: IDSEL
Pin B7: INTB
Pin B8: INTC

USB

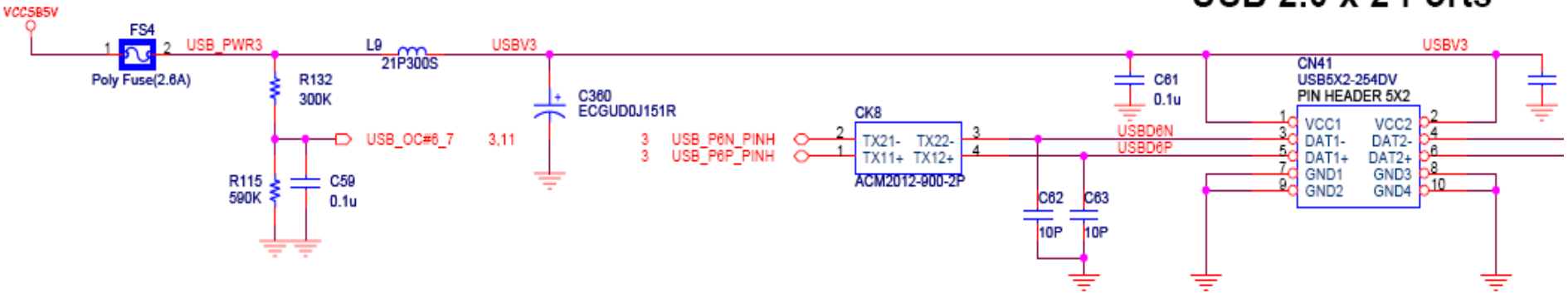
USB connector

USB Connector

USB Connector Signal Description

Signal	Pin	Description	I/O	Comment
VCC	1	+5V Power Supply	P 5V	Must be current-limited for external devices
-DATA	2	Universal Serial Bus Data, negative differential signal.	I/O USB	
+DATA	3	Universal Serial Bus Data, positive differential signal.	I/O USB	
GND	4	Ground	P	

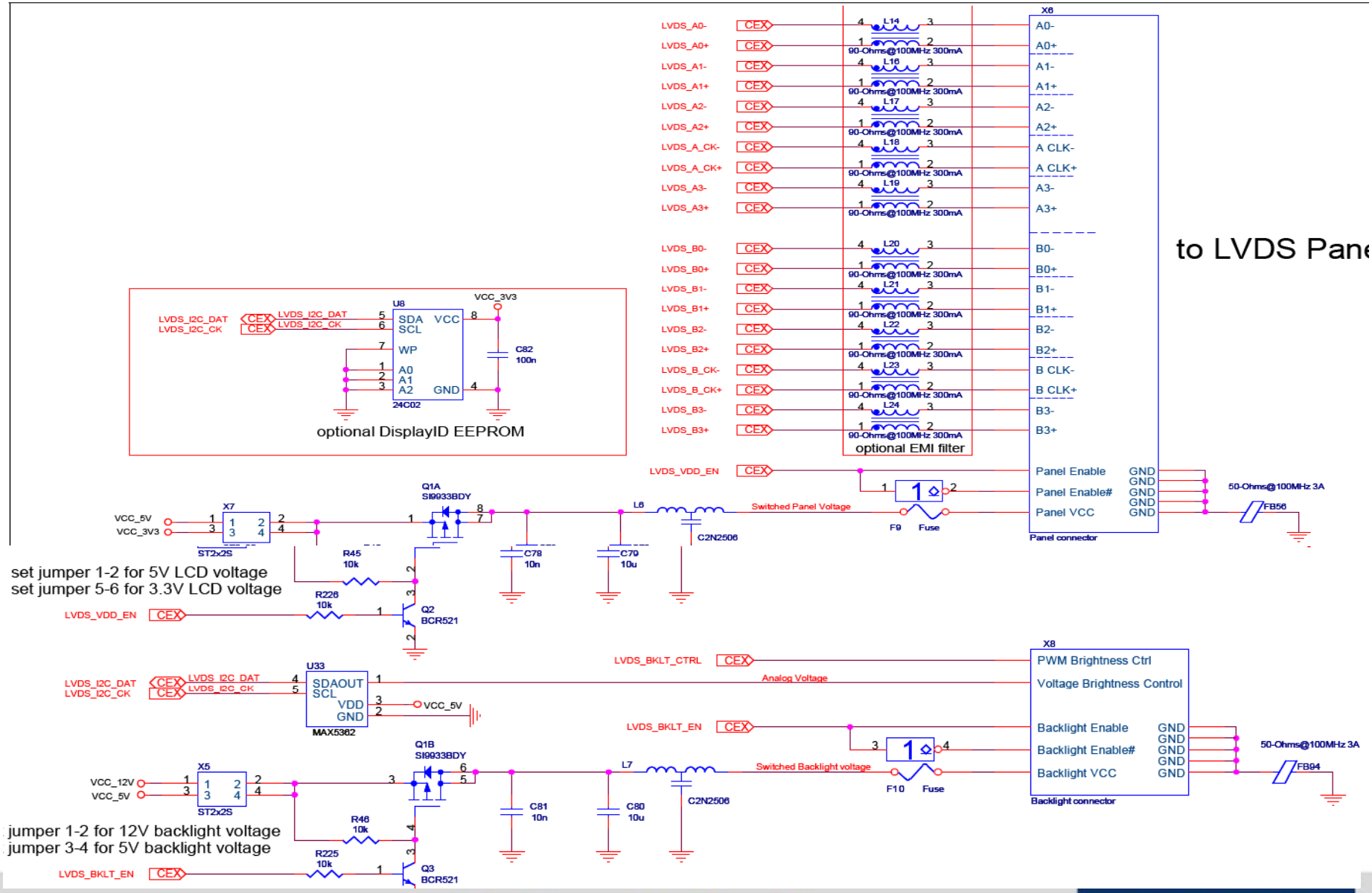
USB 2.0 x 2 Ports



Power to the USB Port is filtered using a ferrite (90 Ω @100MHz, 3000mA) to minimize emissions. The ferrite should be placed adjacent to the USB Port connector pins.

LVDS

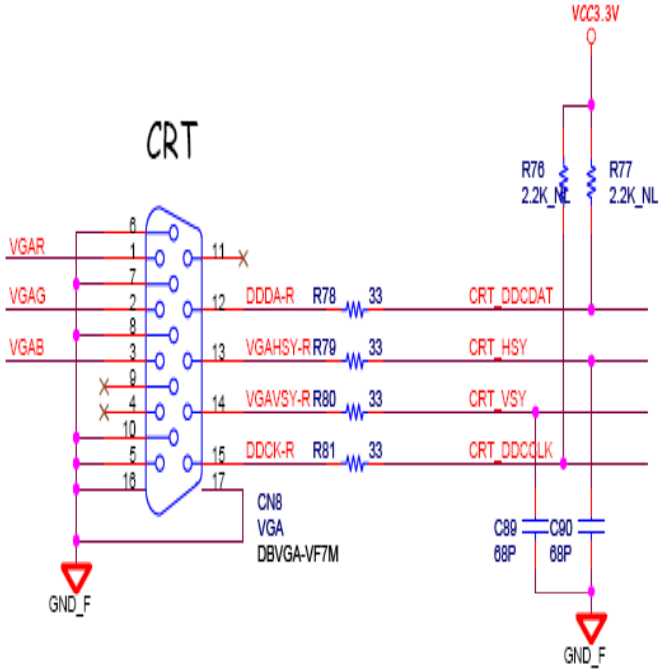
LVDS Reference Schematic



VGA

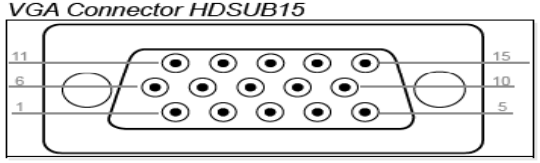
VGA Signal Description

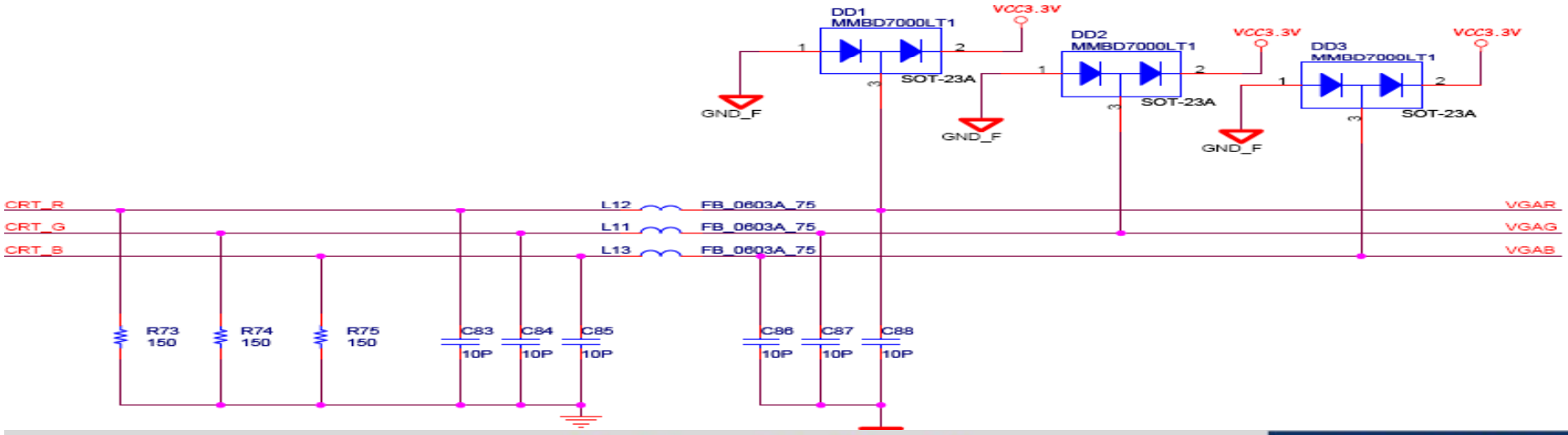
Signal	Pin	HDSUB15	Description	I/O	Comment
VGA_RED	B89	1	Red component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.	O Analog	Analog output
VGA_GRN	B91	2	Green component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.	O Analog	Analog output
VGA_BLU	B92	3	Blue component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.	O Analog	Analog output
VGA_HSYNC	B93	13	Horizontal sync output to VGA monitor.	O 3.3V CMOS	
VGA_VSYNC	B94	14	Vertical sync output to VGA monitor.	O 3.3V CMOS	
VGA_I2C_CK	B95	15	DDC clock line (I2C port dedicated to identify VGA monitor capabilities).	O 3.3V CMOS	
VGA_I2C_DAT	B96	12	DDC data line.	I/O 3.3V CMOS	
GND		5..8, 10	Analog and Digital GND		
DDC_POWER		9	5V DDC supply voltage for monitor EEPROM		Power
N.C.		4, 11	Not Connected		



VGA Connector

VGA Connector HDSUB15





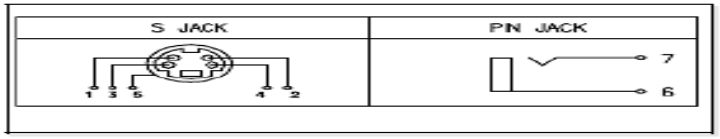
TV-OUT

TV-Out Signal Definitions

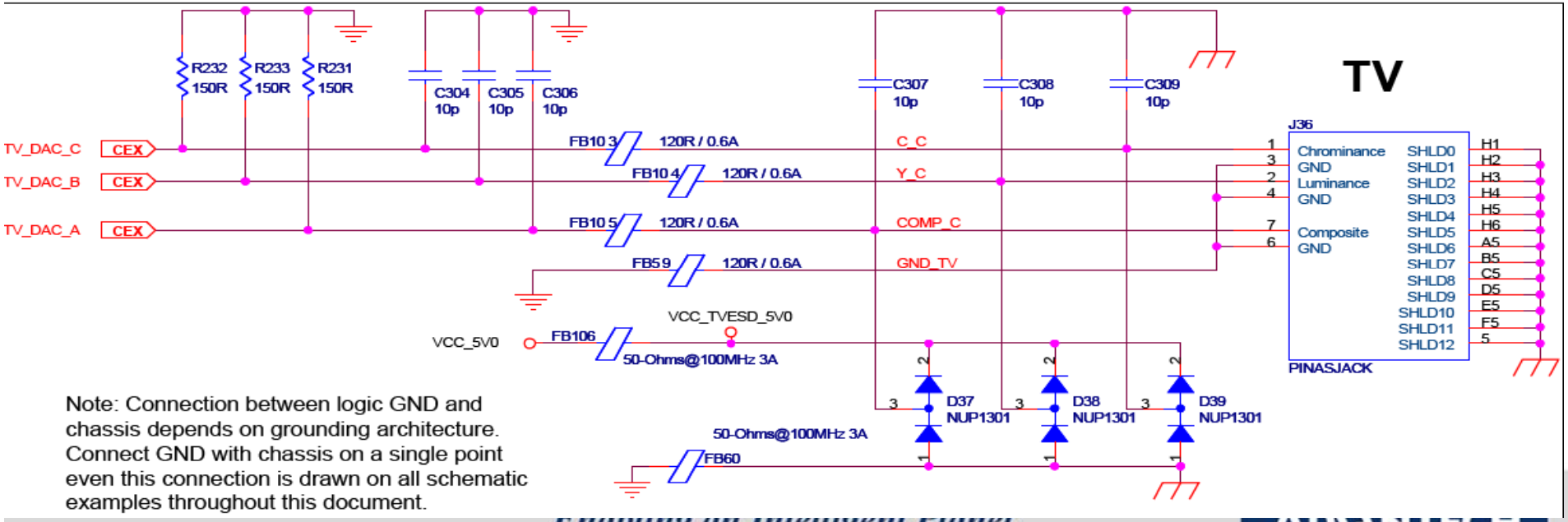
Signal	Pin	Description	I/O	Comment
TV_DAC_A	B97	TV-DAC channel A output supporting: **Composite video**: CVBS **Component video**: Chrominance (Pb) **S-Video**: not used	O Analog	Analog output
TV_DAC_B	B98	TV-DAC channel B output supporting: **Composite video**: not used **Component video**: Luminance (Y) **S-Video**: Luminance (Y)	O Analog	Analog output
TV_DAC_C	B99	TV-DAC channel C output supporting: **Composite video**: not used **Component**: Chrominance (Pr) **S-Video**: Chrominance (C)	O Analog	Analog output

TV-Out Connector

TV-Out Video Connector (combined S-Video and Composite)



TV-Out Reference Schematics



Note: Connection between logic GND and chassis depends on grounding architecture. Connect GND with chassis on a single point even this connection is drawn on all schematic examples throughout this document.

Low Pin Count Interface (LPC)

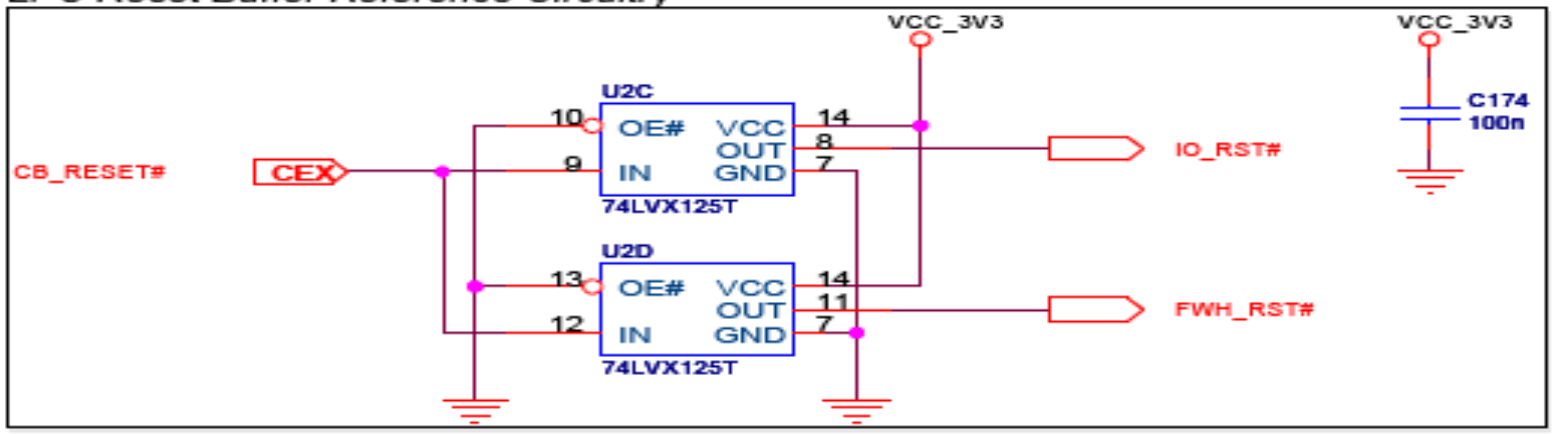
LPC Interface Signal Descriptions

Signal	Pin	Description	I/O	Comment
LPC_SERIRQ	A50	LPC serialized IRQ.	I/O 3.3V CMOS	
LPC_FRAME#	B3	LPC frame indicates start of a new cycle or termination of a broken cycle.	O 3.3V CMOS	
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B4 B5 B6 B7	LPC multiplexed command, address and data.	I/O 3.3V CMOS	
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC encoded DMA/Bus master request.	I 3.3V CMOS	Not all modules support LPC DMA. Contact your vendor for information.
LPC_CLK	B10	LPC clock output 33MHz.	O 3.3V CMOS	

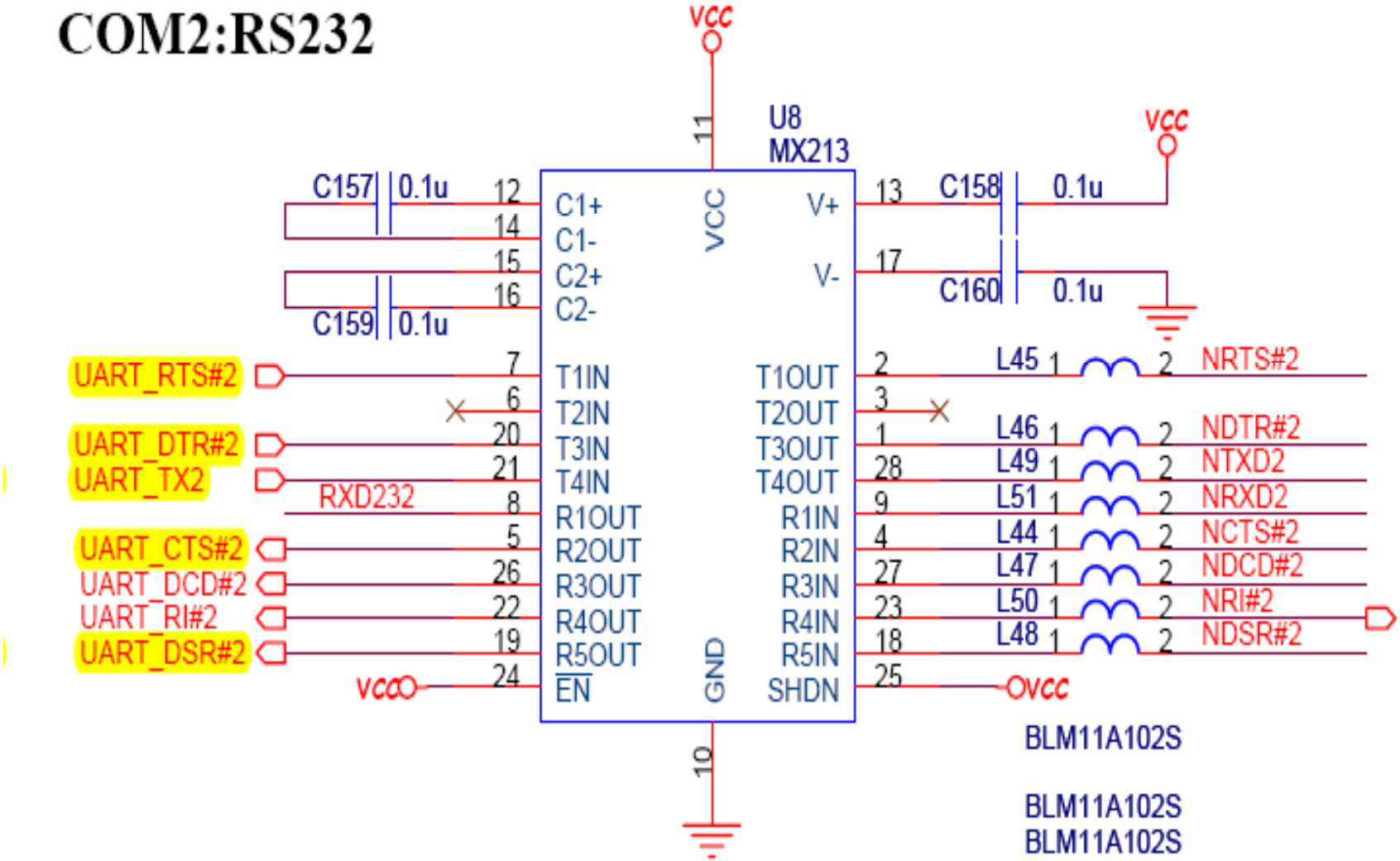
LPC Reset Signal

The LPC interface should use the signal 'CB_RESET#' as its reset input. This signal is issued by the COM Express Module as a result of a low 'SYS_RESET#', a low 'PWR_OK' or a watchdog timeout event. If there are multiple LPC devices implemented on the Carrier Board, it is recommended to split the signal 'CB_RESET#' so that each LPC device will be provided with a separate reset signal. Therefore a buffer circuit like the one shown in Figure 37 below should be used.

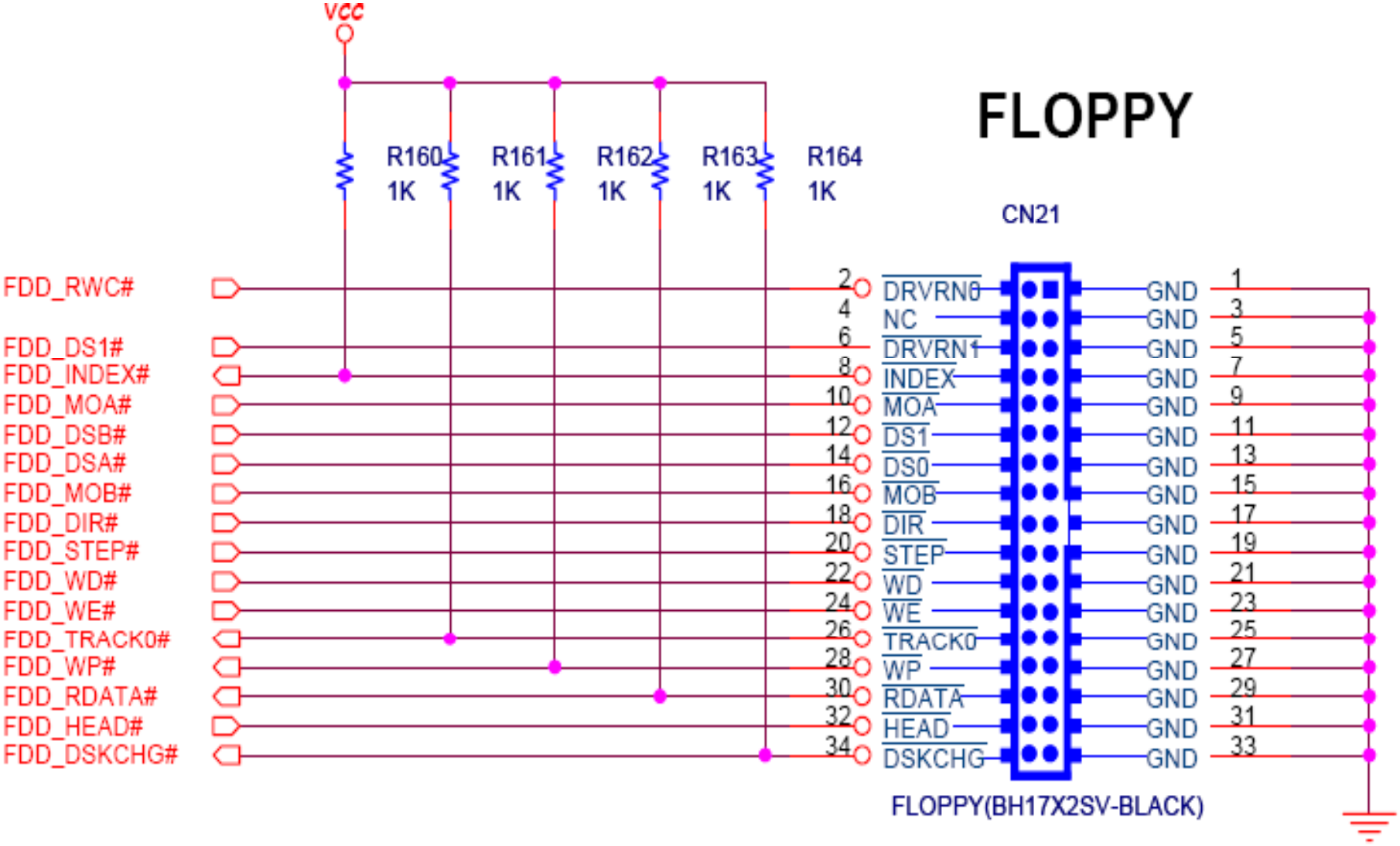
LPC Reset Buffer Reference Circuitry



COM Port

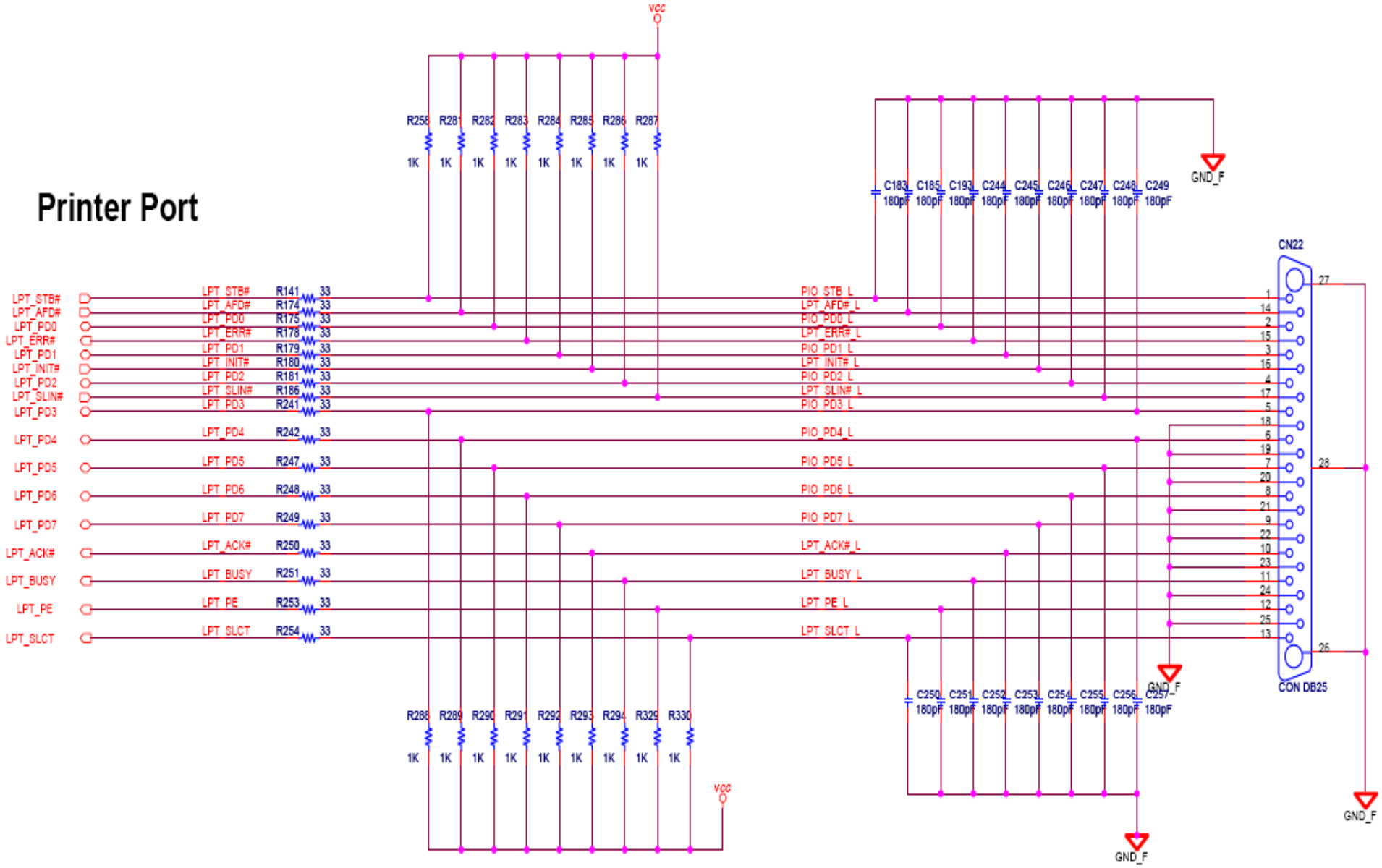

COM2:RS232
VCC
U8
MX213
C157
0.1u
C159
0.1u
C158
0.1u
C160
0.1u
C1+
C1-
C2+
C2-
VCC
V+
V-
T1IN
T2IN
T3IN
T4IN
R1OUT
R2OUT
R3OUT
R4OUT
R5OUT
EN
GND
T1OUT
T2OUT
T3OUT
T4OUT
R1IN
R2IN
R3IN
R4IN
R5IN
SHDN
UART_RTS#2
UART_DTR#2
UART_TX2
RXD232
UART_CTS#2
UART_DCD#2
UART_RI#2
UART_DSR#2
VCCO
OVCC
L45
L46
L49
L51
L44
L47
L50
L48
NRTS#2
NDTR#2
NTXD2
NRXD2
NCTS#2
NDCD#2
NRI#2
NDSR#2
BLM11A102S
BLM11A102S
BLM11A102S

FLOPPY

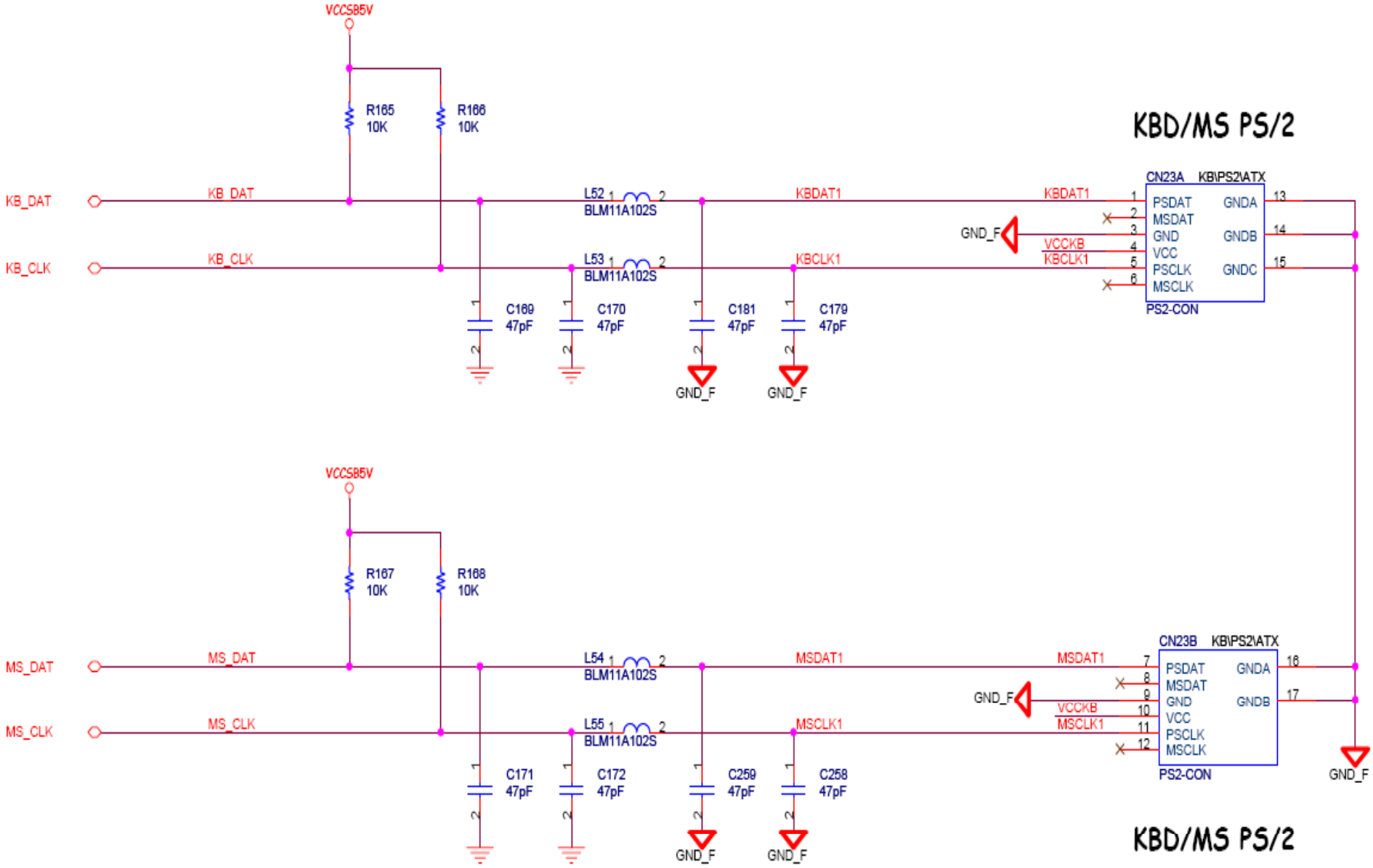

VCC
R160 1K
R161 1K
R162 1K
R163 1K
R164 1K
FLOPPY
CN21
FDD_RWC#
FDD_DS1#
FDD_INDEX#
FDD_MOA#
FDD_DSB#
FDD_DSA#
FDD_MOB#
FDD_DIR#
FDD_STEP#
FDD_WD#
FDD_WE#
FDD_TRACK0#
FDD_WP#
FDD_RDATA#
FDD_HEAD#
FDD_DSKCHG#
2 DRVRN0
4 NC
6 DRVRN1
8 INDEX
10 MOA
12 DS1
14 DS0
16 MOB
18 DIR
20 STEP
22 WD
24 WE
26 TRACK0
28 WP
30 RDATA
32 HEAD
34 DSKCHG
GND 1
GND 3
GND 5
GND 7
GND 9
GND 11
GND 13
GND 15
GND 17
GND 19
GND 21
GND 23
GND 25
GND 27
GND 29
GND 31
GND 33
FLOPPY(BH17X2SV-BLACK)

Printer

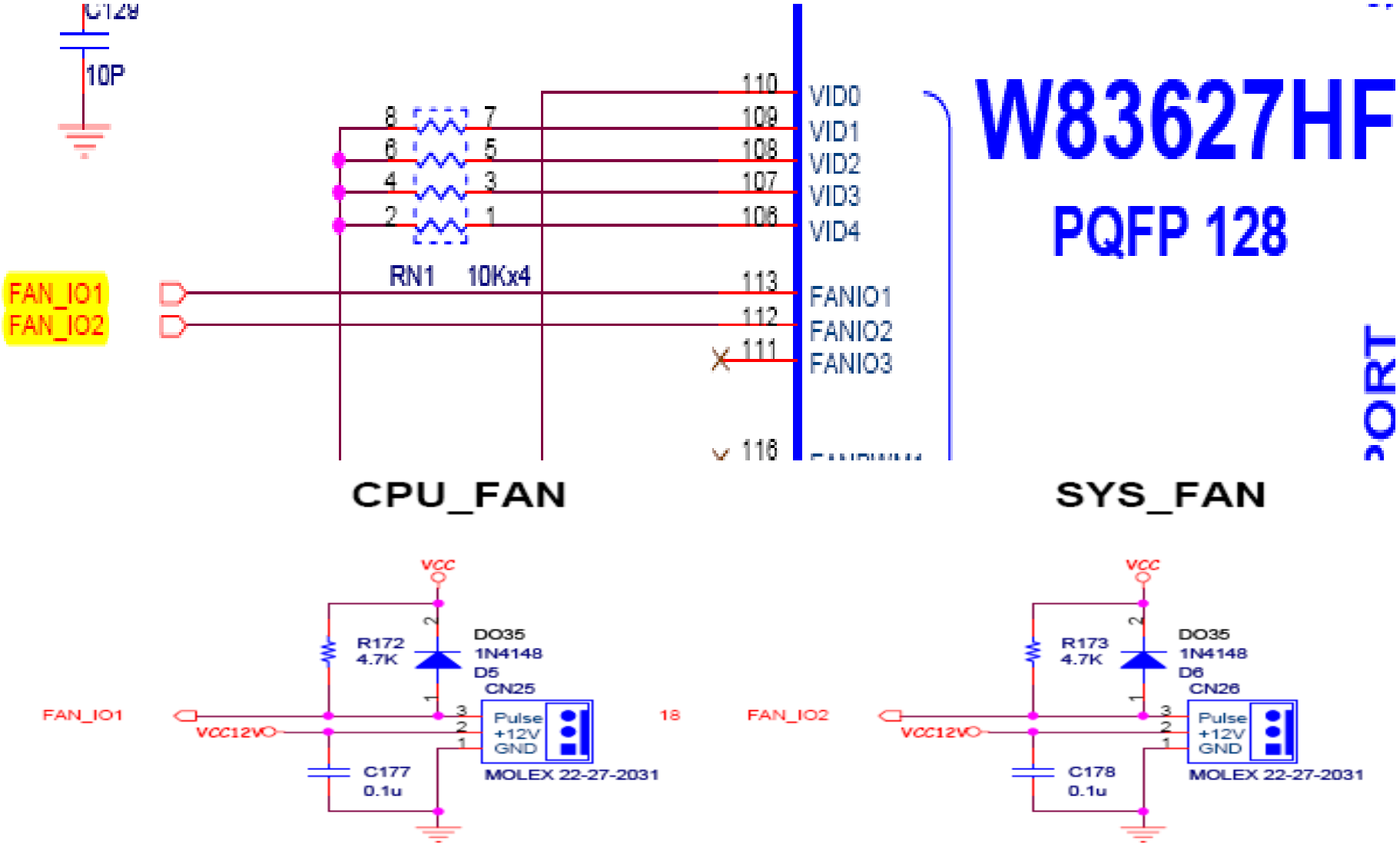
Printer Port



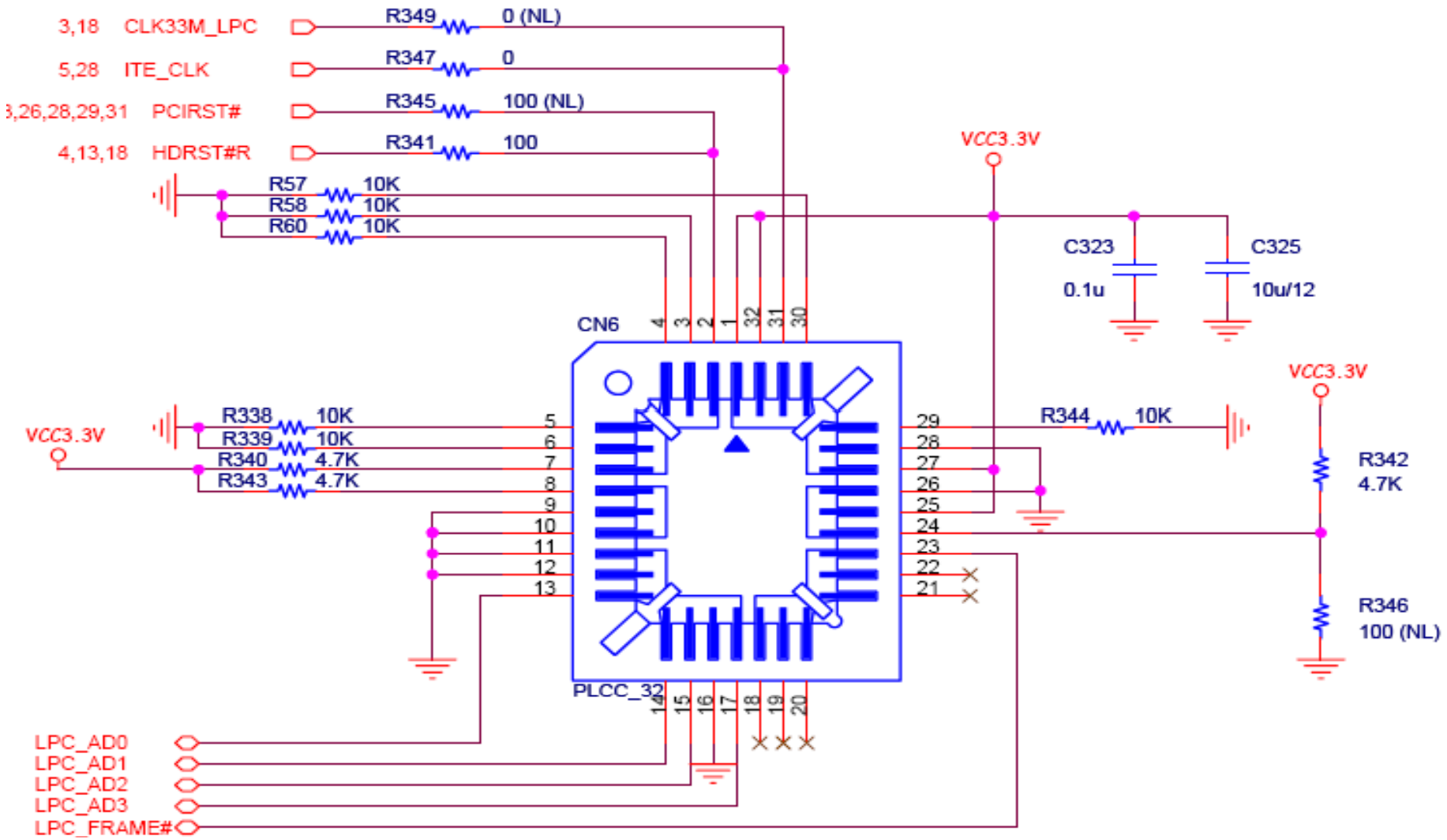
PS2 Port


VCCSB5V
R165
10K
R166
10K
KBD/MS PS/2
KB_DAT
KB_DAT
KB_CLK
KB_CLK
L52
BLM11A102S
L53
BLM11A102S
KBDAT1
KBCLK1
CN23A KB\PS2\ATX
PSDAT
MSDAT
GND
VCC
PSCLK
MSCLK
GNDA
GNDB
GNDC
PS2-CON
GND_F
VCCKB
C169
47pF
C170
47pF
C181
47pF
C179
47pF
VCCSB5V
R167
10K
R168
10K
MS_DAT
MS_DAT
MS_CLK
MS_CLK
L54
BLM11A102S
L55
BLM11A102S
MSDAT1
MSCLK1
CN23B KB\PS2\ATX
PSDAT
MSDAT
GND
VCC
PSCLK
MSCLK
GNDA
GNDB
PS2-CON
GND_F
VCCKB
C171
47pF
C172
47pF
C259
47pF
C258
47pF
KBD/MS PS/2

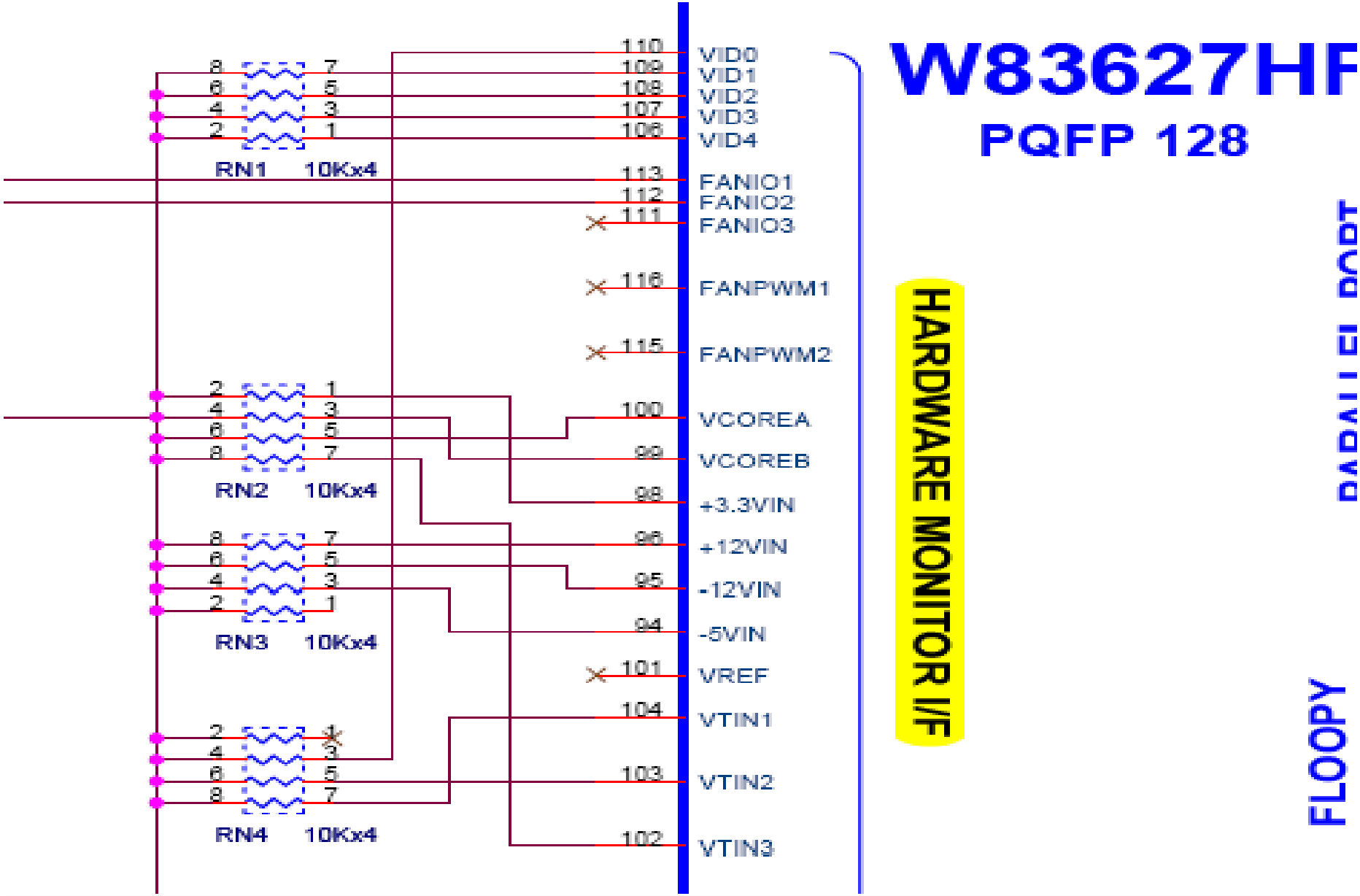
FAN Control


10P
FAN_IO1
FAN_IO2
RN1 10Kx4
VID0
VID1
VID2
VID3
VID4
FANIO1
FANIO2
FANIO3
W83627HF
PQFP 128
CPU_FAN
SYS_FAN
VCC
R172
4.7K
DO35
1N4148
D5
CN25
Pulse
+12V
GND
MOLEX 22-27-2031
VCC12V
C177
0.1u
R173
4.7K
D6
CN26
C178
0.1u

BIOS Socket


3,18 CLK33M_LPC
5,28 ITE_CLK
3,26,28,29,31 PCIRST#
4,13,18 HDRST#R
R349 0 (NL)
R347 0
R345 100 (NL)
R341 100
R57 10K
R58 10K
R60 10K
VCC3.3V
C323
0.1u
C325
10u/12
CN6
PLCC_32
R338 10K
R339 10K
R340 4.7K
R343 4.7K
R344 10K
R342
4.7K
R346
100 (NL)
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#

HWM Function

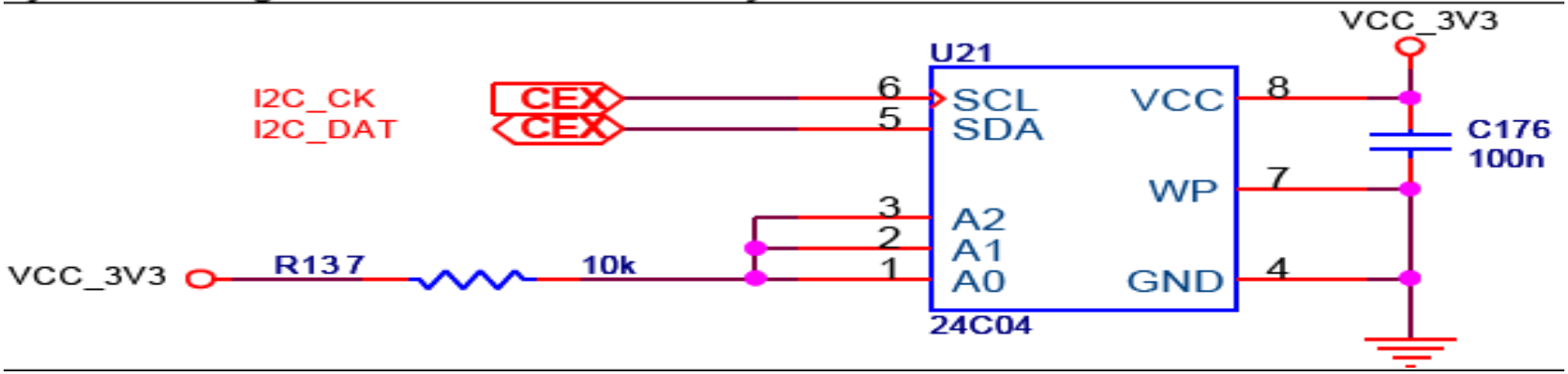


Miscellaneous (MICS)

General Purpose I2C Interface Signal Descriptions

Signal	Pin	Description	I/O	Pwr Rail	Comment
I2C_CK	B33	General Purpose I2C Clock output	O CMOS	3.3V	
I2C_DAT	B34	General Purpose I2C data I/O line.	I/O OD CMOS	3.3V	

System Configuration EEPROM Circuitry



Routing Considerations

The maximum amount of capacitance allowed on the Carrier General Purpose I2C bus lines (I2C_DAT, I2C_CK) is specified by your Module vendor. The Carrier designer is responsible for ensuring that the maximum amount of capacitance is not exceeded and the rise/fall times of the signals meet the I2C bus specification. As a general guideline, an IC input has 12pF of capacitance, and a PWB trace has 3.8pF per inch of trace length. Do not connect Standby Power to I2C devices unless bus isolation is used to prevent back feeding of voltage from the Suspend supply to the Non-Suspend supply voltages.

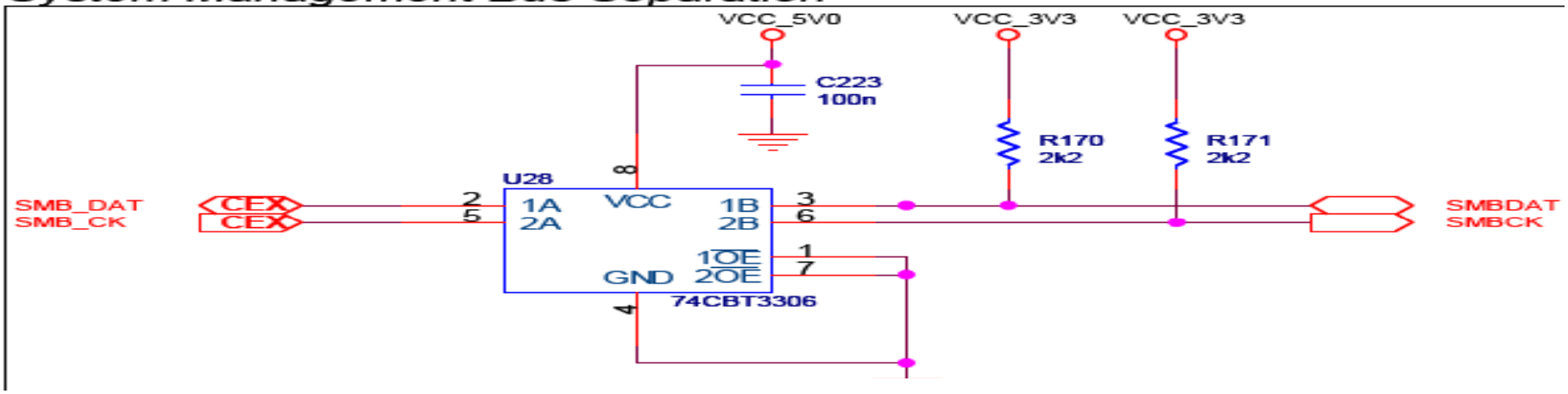
SMBUS

Signal Definitions

System Management Bus Signals

Signal	Pin	Description	I/O	Pwr Rail	Comment
SMB_CK	B13	System Management Bus bidirectional clock line	I/O OD CMOS	3.3V Suspend rail	
SMB_DAT	B14	System Management bidirectional data line.	I/O OD CMOS	3.3V Suspend rail	
SMB_ALERT#	B15	System Management Bus Alert	I CMOS	3.3V Suspend Rail	

System Management Bus Separation



Routing Considerations

SMBus should be connected to all or none of the PCIe/PCI devices and slots. A general recommendation is to not connect these devices to the SMBus.

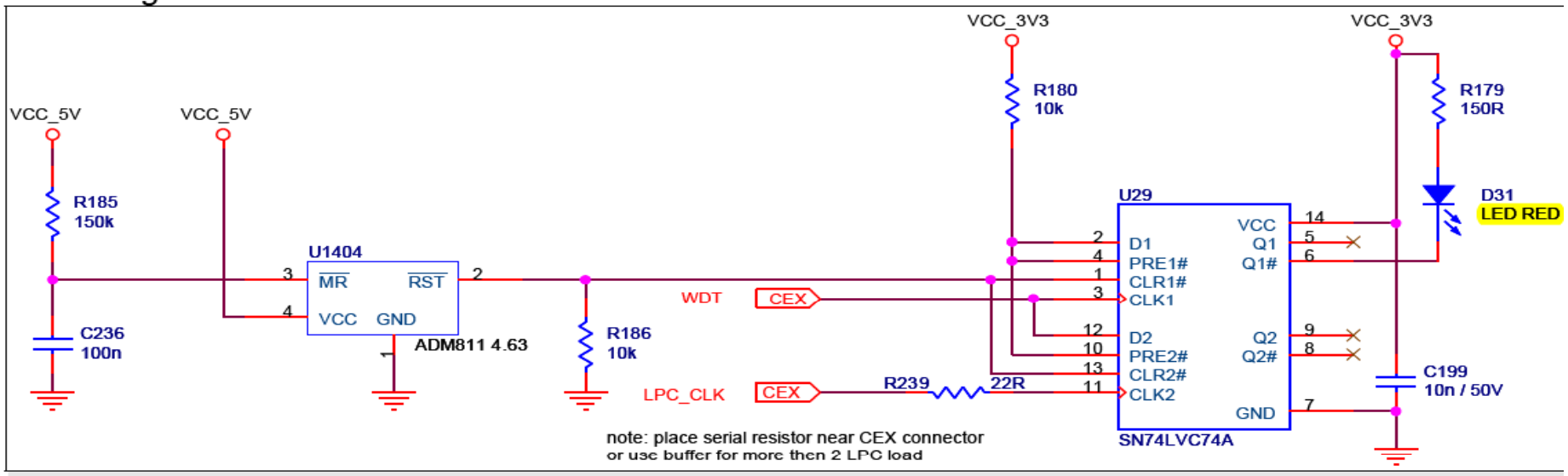
The maximum load of SMBus lines is limited to 3 external devices. Please contact your module vendor if more devices are required.

Do not connect Non-Suspend powered devices to the SMBus unless a bus switch is used to prevent back feeding of voltage from the Suspend rail to other supplies.

Contact your Module vendor for a list of SMBus addresses used on the Module. Do not use the same address for Carrier located devices.

Watchdog Timer

Watchdog Timer Event Latch Schematic



The Watchdog Timer (WDT) event signal is provided by the COM Express Module. The WDT output is active-high. It is sourced from Module pin B27.

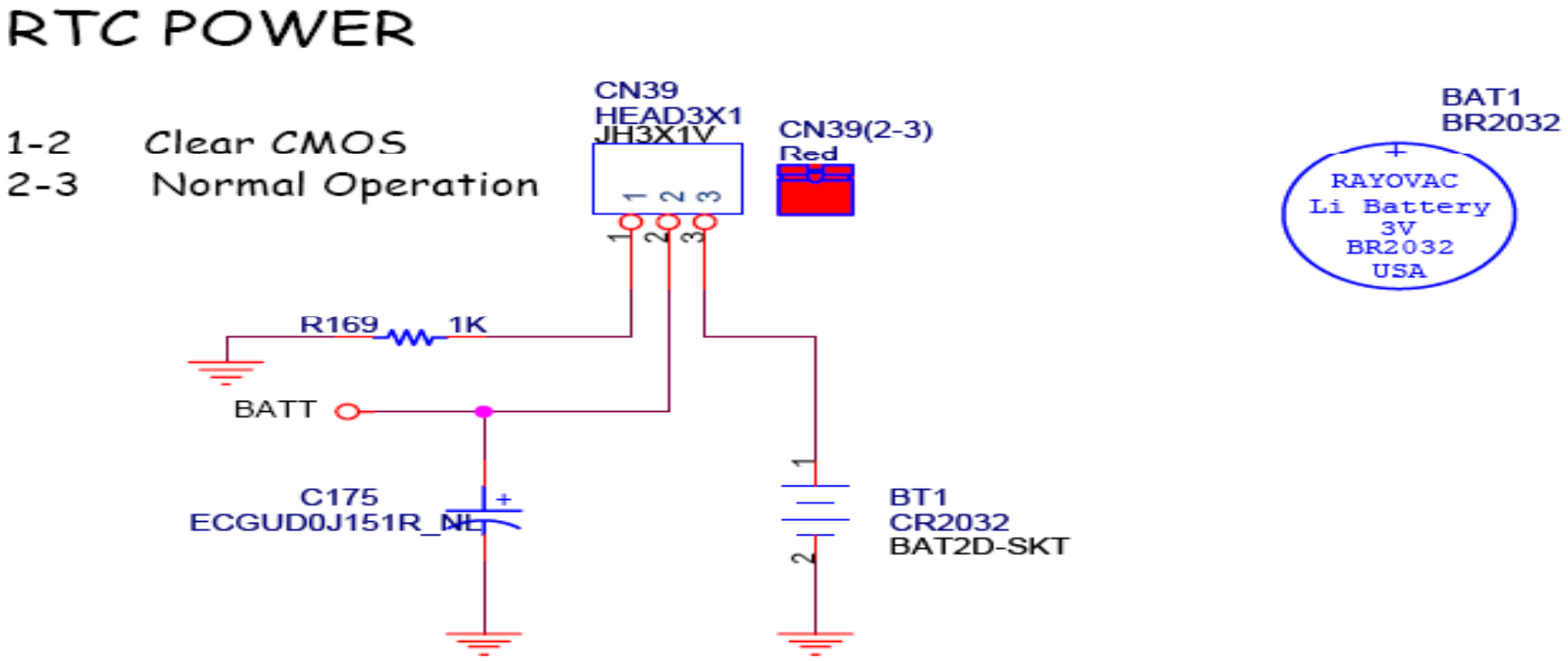
The WDT event can cause the system to reset by making appropriate Carrier Board connections. It also may be possible to configure the Module to reset on a WDT event; check the manufacturer's Module Users Guide.

If the WDT output is used to cause a system reset, the WDT output will be cleared by the system reset event.

The WDT can be latched to drive a LED for a visual indication of an event, as shown in this example. Note that the latch is powered by a power rail that is active in all power states, including the soft-off state. The latch is only cleared by a complete power cycle. The cold power-up cycle is signaled by the RSMRST# net (Resume Reset, active low). A Carrier Board reset monitor, not shown in this figure, is required to generate the RSMRST# signal. The reset monitor should monitor the 5V or 3.3V Suspend power rail (V5.0_S5 or V3.3_S5).

RTC

A47	VCC_RTC	Power		Real-time clock circuit-power input. Nominally +3.0V. See Electrical Specifications section for details.	Connect 1KΩ in series to 3.3V Battery	Connect 1KΩ in series to 3.3V Battery



General Purpose Input/Output (GPIO)

GPIO Signal Definition

Signal	Pin	Description	I/O	Comment
GPI0	A54	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS	
GPI1	A63	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS	
GPI2	A67	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS	
GPI3	A85	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS	
GPO0	A93	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V CMOS	
GPO1	B54	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V CMOS	
GPO2	B57	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V CMOS	
GPO3	B63	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V CMOS	

There are 4 GPI (General Purpose Inputs) and 4 GPO (General Purpose Outputs) pins in Figure 49 above.

The signals drive switch inputs such as Lamps, Relays, and Sensors.

GPI signals from a header are shown with protection diodes. The signals are connected for input to the COM Express Module.

GPO signals from the COM Express Module are shown buffered. The signals are connected to the header with protection diodes.

Power Supply

A97~A99,A101~A109 B101~B109 C104~C109 D104~D109	VCC_12V	Power		Primary power input: +12V nominal. See Electrical Specifications section for allowable input range. All available VCC_12V pins on the connector(s) **shall** be used.	Connect to 12V	Connect to 12V
B84~B87	VCC_5V_SBY	Power		Standby power input: +5.0V nominal. See Electrical Specifications section for allowable input range. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) **shall** be used. Only used for standby and suspend functions. **May** be left unconnected if these functions are not used in the system design.	ATX - Connect to 5VSB AT - N/C	ATX - Connect to 5VSB AT - N/C

ATX Signal Names

ATX Signal Name	Description
PS_ON#	Active-low, TTL-level input to ATX supply that, when low, enables all power rails. If high or floating, all ATX power rails are disabled except for the +5V Suspend rail.
PWR_OK	Active-high, TTL-level output signal from the ATX supply that indicates that the +12V, +5V, +3.3V and -12V outputs are all present and OK to use.
+12V1DC	+12V power rail for use by all system components except for the CPU, controlled by PS_ON#
+12V2DC	+12V power rail for use by the CPU, controlled by PS_ON#. This power rail appears on a separate 2x2 connector for CPU use only.
+5VDC	+5V power rail, controlled by PS_ON#
+3.3VDC	+3.3V power rail, controlled by PS_ON#
-12VDC	-12V power rail, controlled by PS_ON#
+5VSB	+5V Suspend power rail, present whenever the ATX supply is connected to its AC power input source.
COM	Common return path – usually referred to as "ground" or GND

ATX Power Supply Design

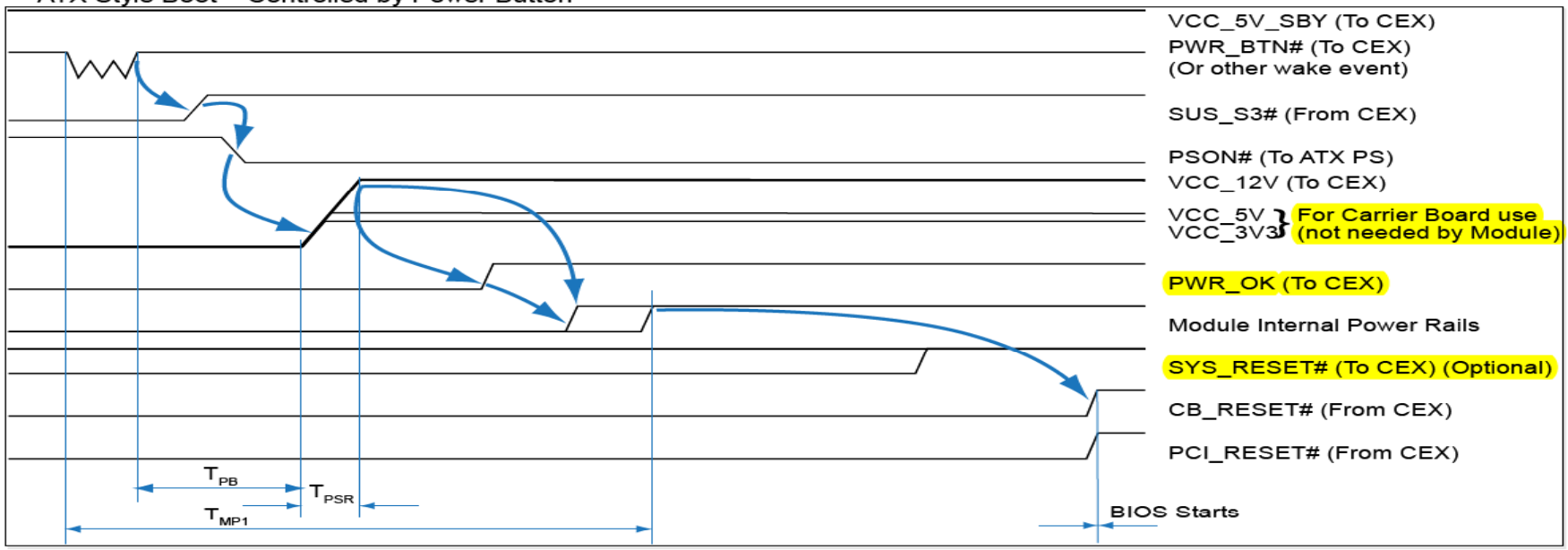
VCC5_SBY Routing

The +5V Suspend power rail, if used, should be sized to handle 2A. Most, but not all, Modules will use considerably less than 2A for this power rail. Modules with multiple Ethernet channels and wake-on-LAN capability will use more current. The COM Express Specification allows up to 2A on this rail.

VCC_5V_SBY tolerance为4.75~~5.25V

VCC_12V tolerance为11.4~~12.6V

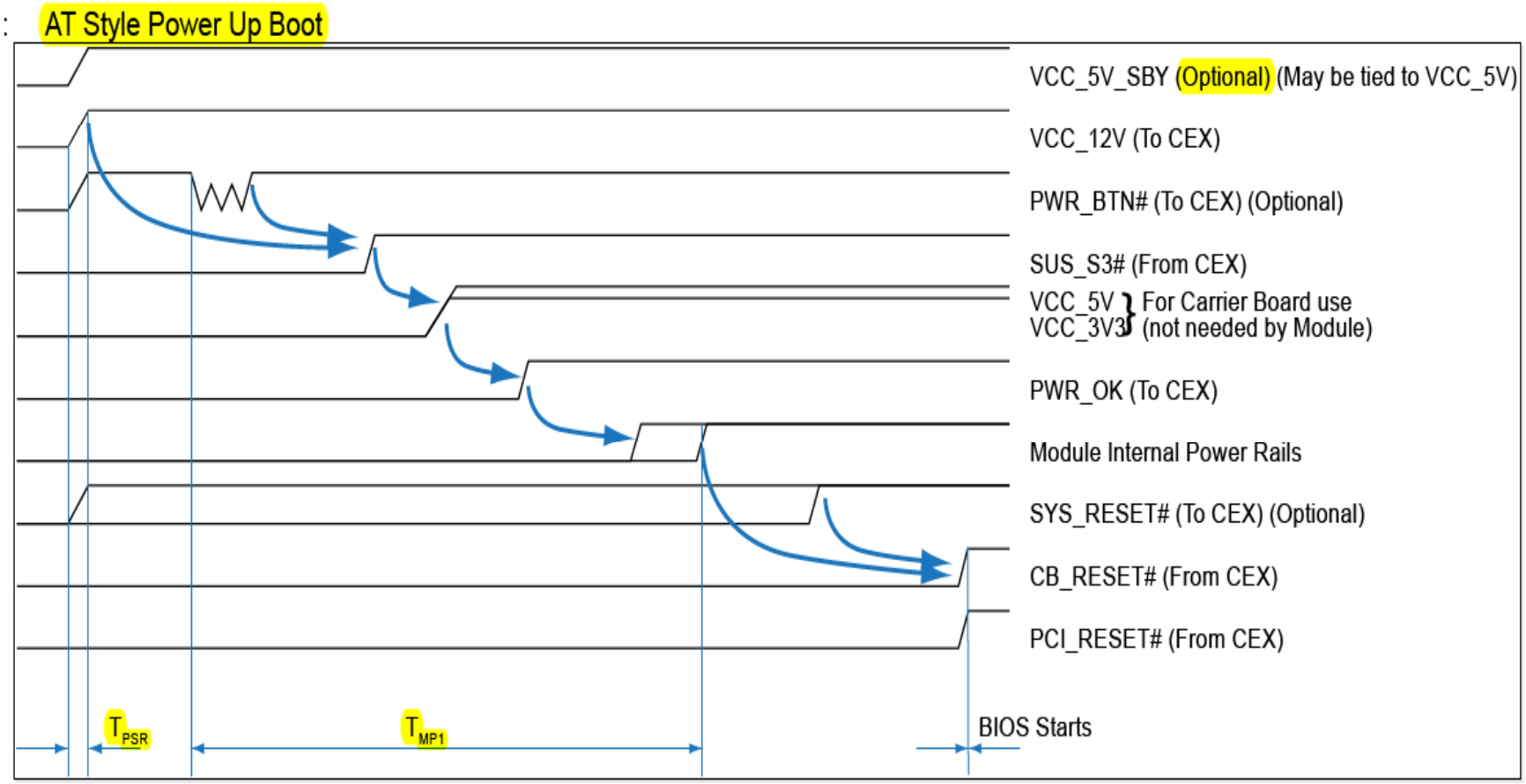
ATX Style Boot – Controlled by Power Button



AT Power Supply Design

1、Remove 5VSB Power,Only VCC_12V Input

2、将BIOS Default 选项Restore AC Power Loss由off变为On



BIOS Considerations

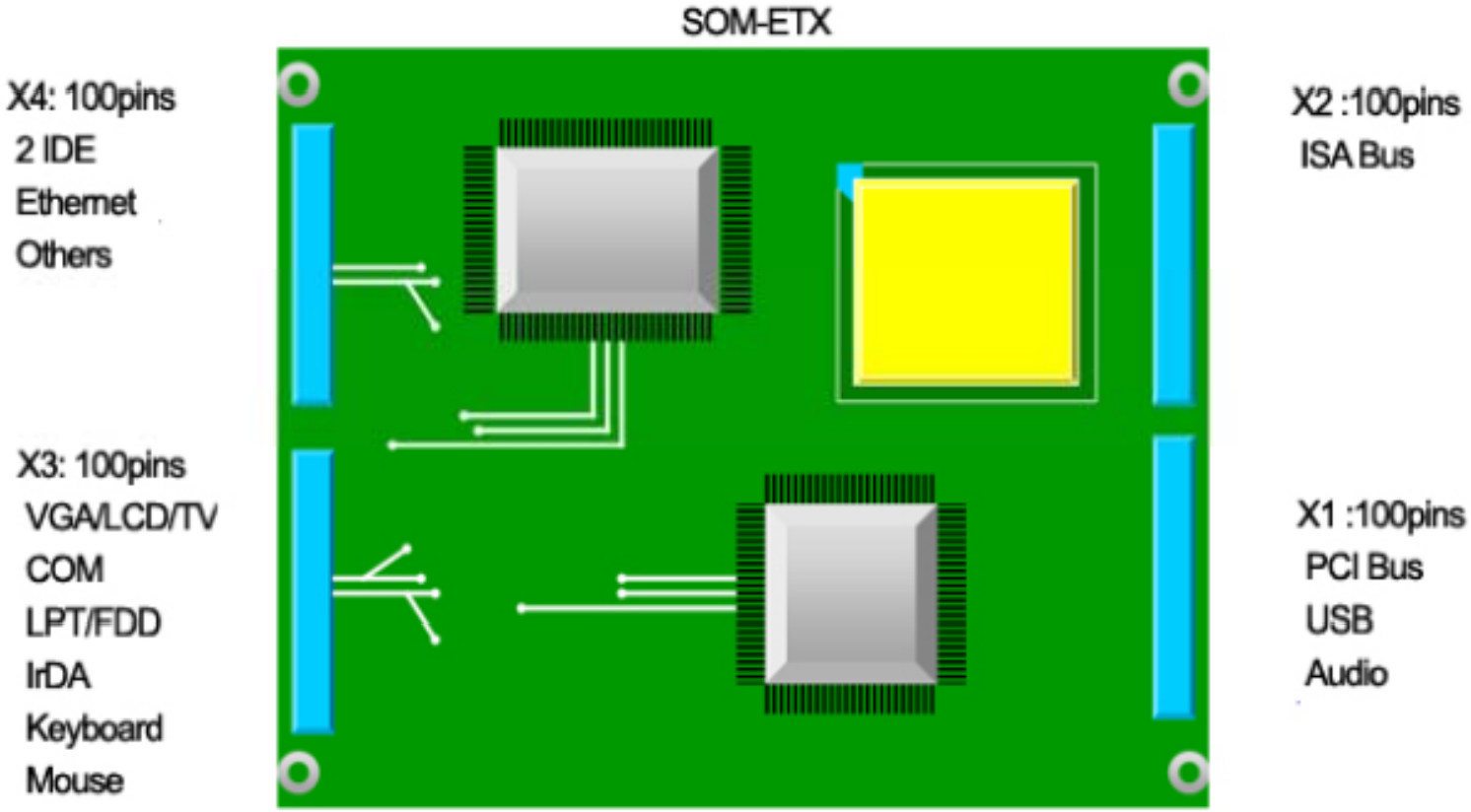
请客户帮忙给出详细的BIOS Request Form给到研华Sales或Local FAE

- 研华标准版本BIOS为Winbond 83627HF,如SIO型号与其不符，请提前告知具体型号，以完成客制化需求

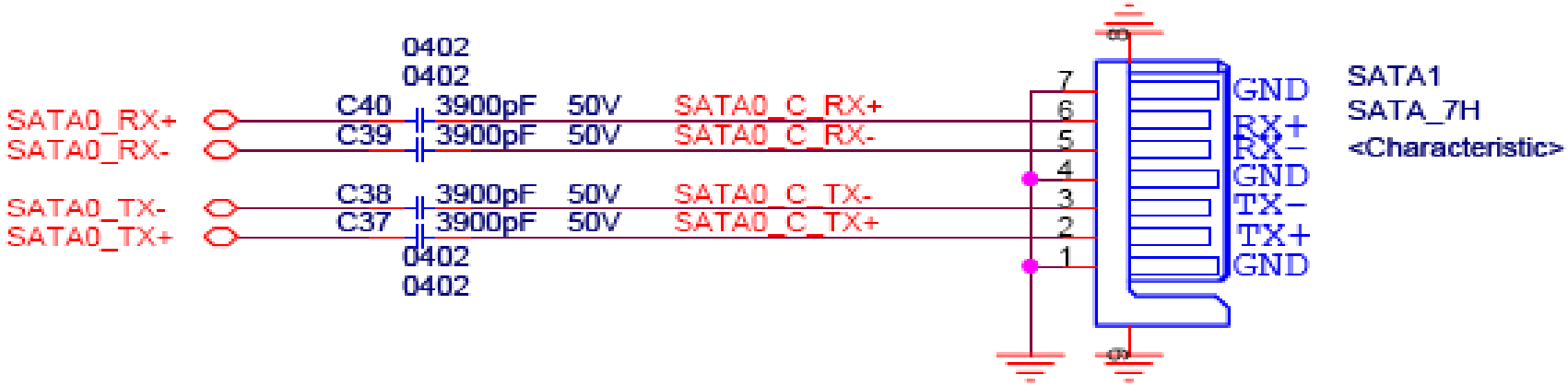
- 如需要增加LOGO，电池管理等功能，请客户提供LOGO图片.jpg 640X480和电池充电芯片的型号及相关Datasheet

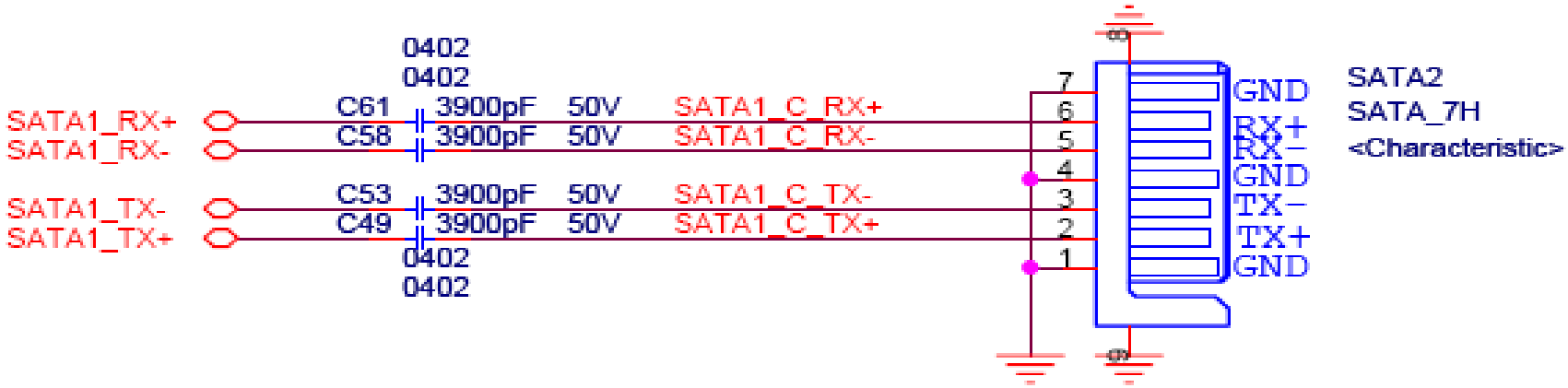
ETX3.0 Form Factor

This chapter describes pin assignments and I/O characteristics for 400 pins SOM-ETX (X1, X2, X3 and X4). X1 connector contains PCI-Bus, USB, Audio interfaces. X2 connector contains ISA-Bus. X3 connector contains VGA, LCD/LVDS, COM1/2, LPT/Floppy, IrDA, KB/MS and TV-Out interfaces. X4 connector contains IDE1, IDE2, Ethernet and miscellaneous.



SATA

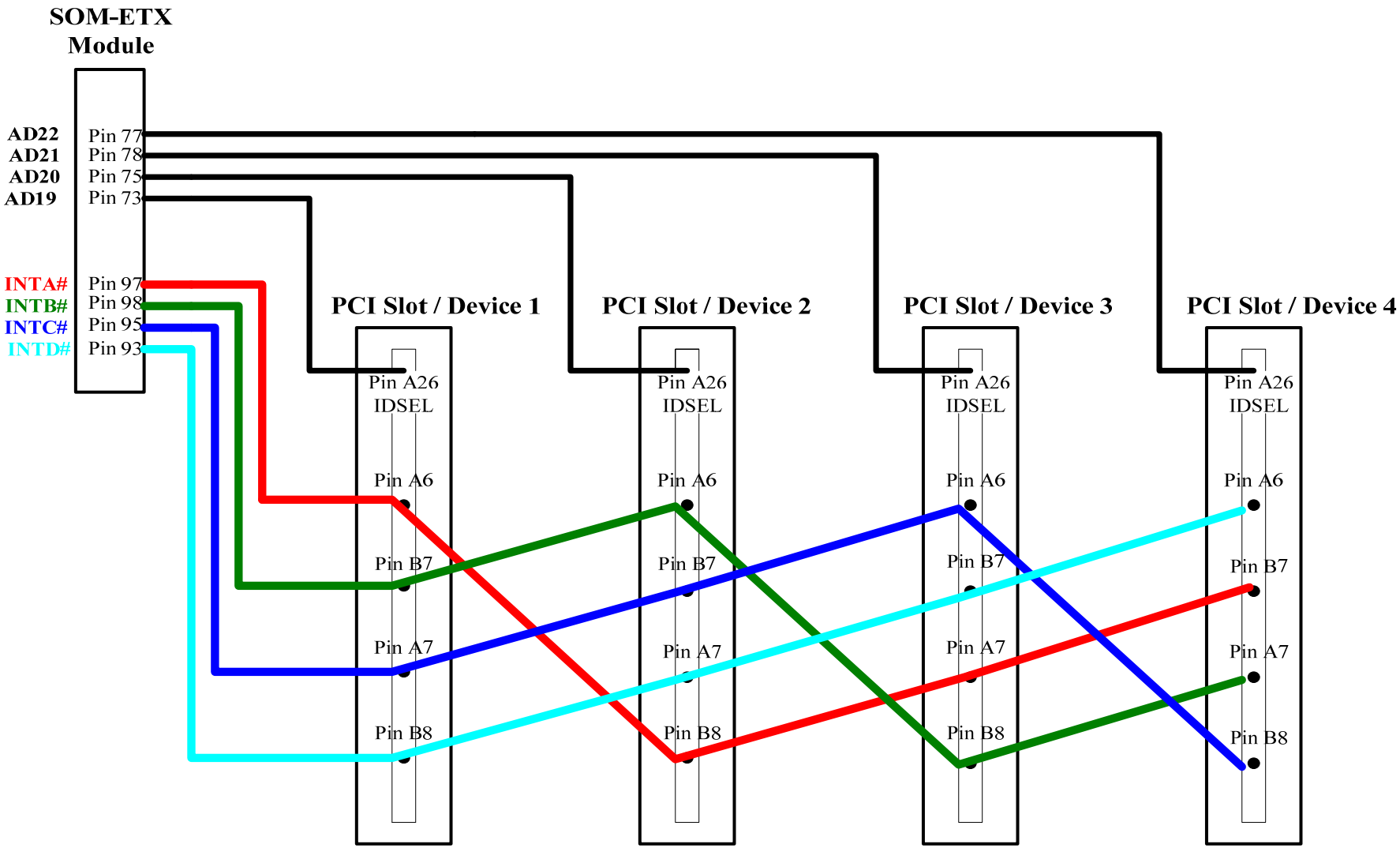




自身提供2个SATA Port，可供客户直接使用

PCI

提供4组PCI Routing

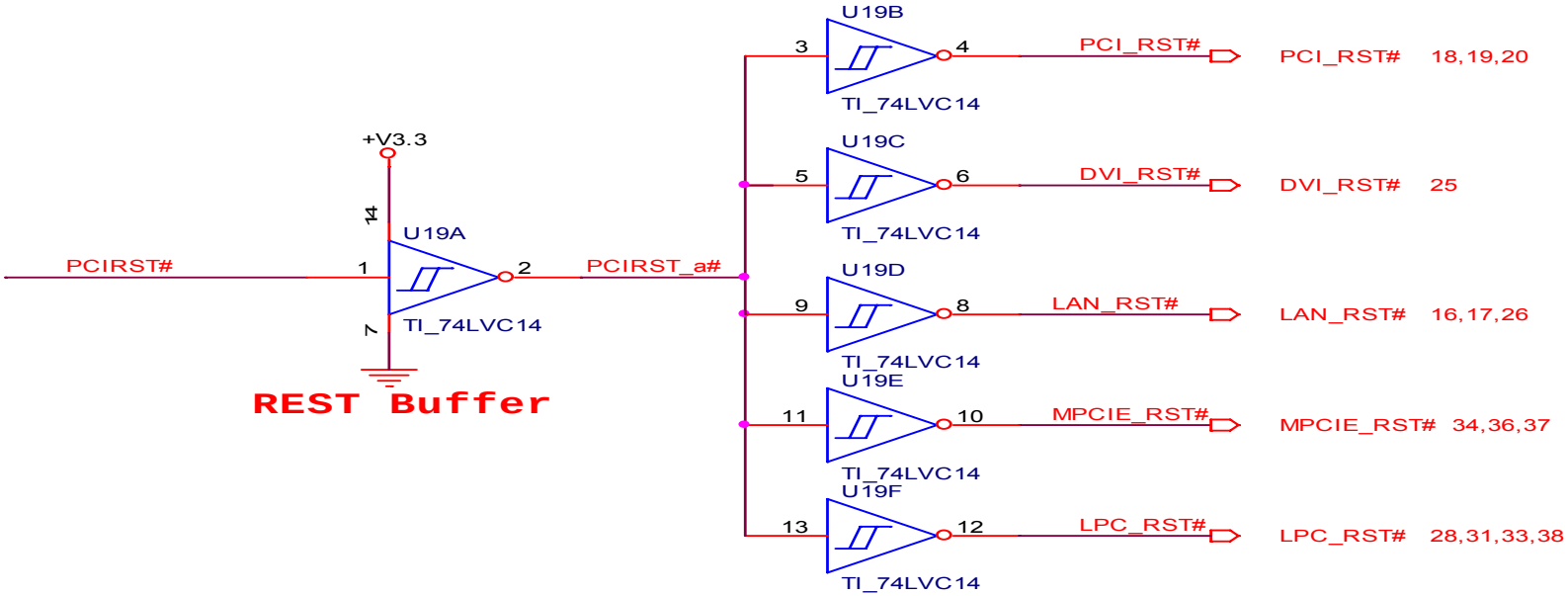


PCI Address（IDSEL)

ETX PCI Routing					
IDSEL	INT#	PCI Device	SOM-4481/4486 A3	SOM-4477	SOM-4455
AD13	INTC#	On board PCI			
AD14	INTD#				
AD15	INTA#				VT6421L
AD16	INTB#		IT8888G	RTL8100CL (INT#C)	82551ER/ RTL8100CL
AD19	INTA#	Carrier board PCI			
AD20	INTB#				
AD21	INTC#				
AD22	INTD#				

PCI Resource

PCI Sequence :3组以上PCI设备建议增加 Reset buffer和Clk Buffer



PCI Clock:要求两设备间的时间差不超过2ns，所以PCI clock尽量拉等长

Table 4-8: Clock Skew Parameters

Symbol	5V Signaling	3.3V Signaling	Units
V_{test}	1.5	0.4 V_{CC}	V
T_{skew}	2 (max)	2 (max)	ns

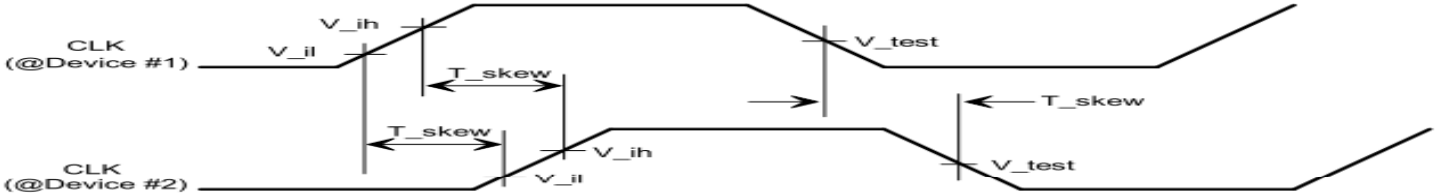
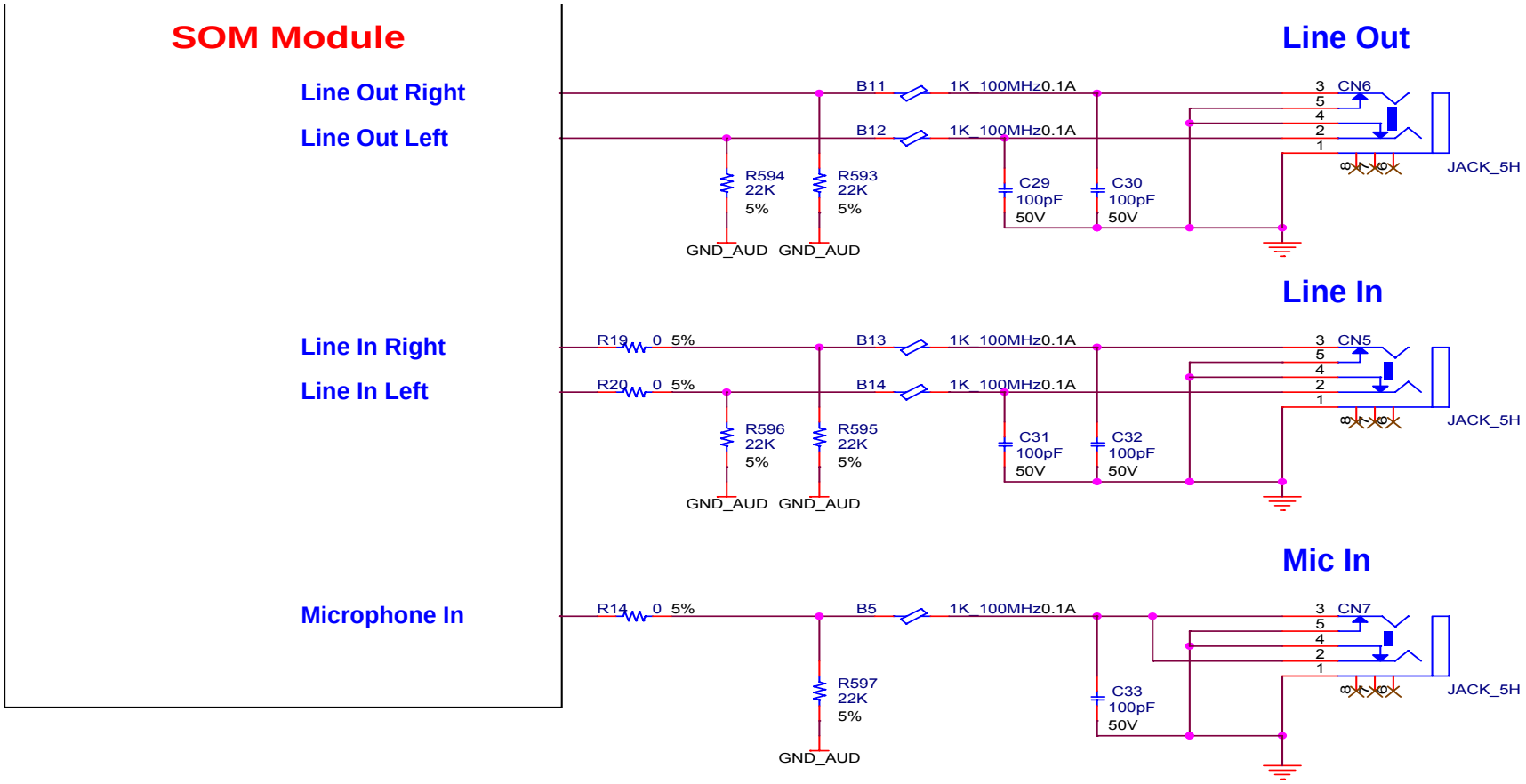


Figure 4-11: Clock Skew Diagram

Audio

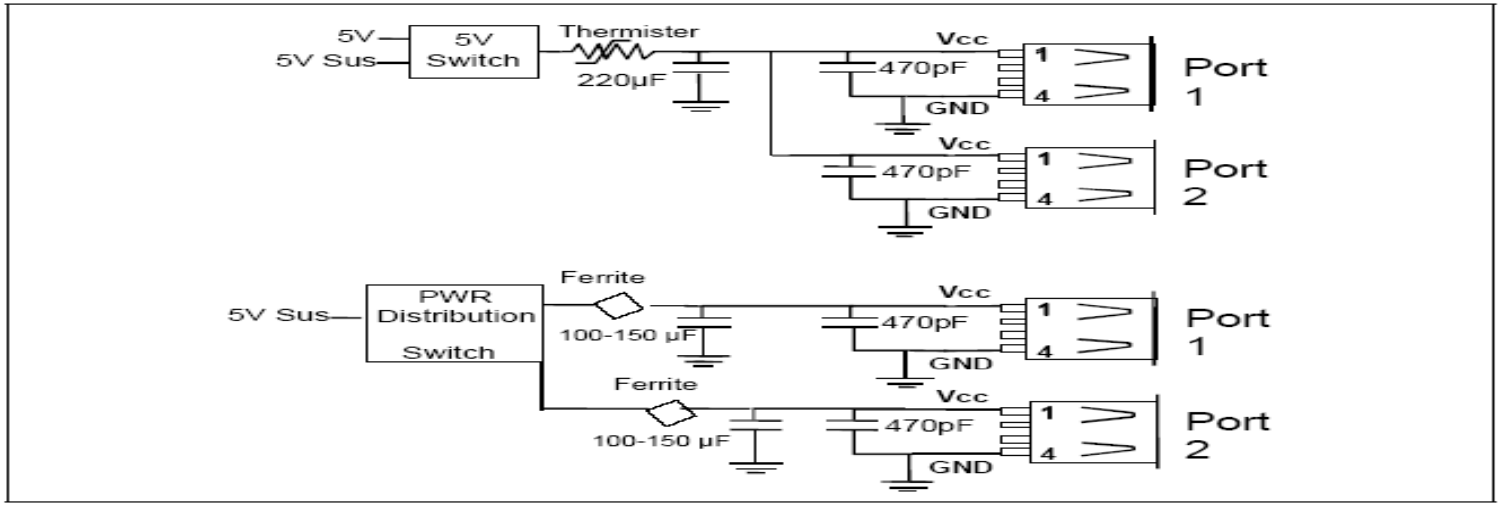
Schematic Design

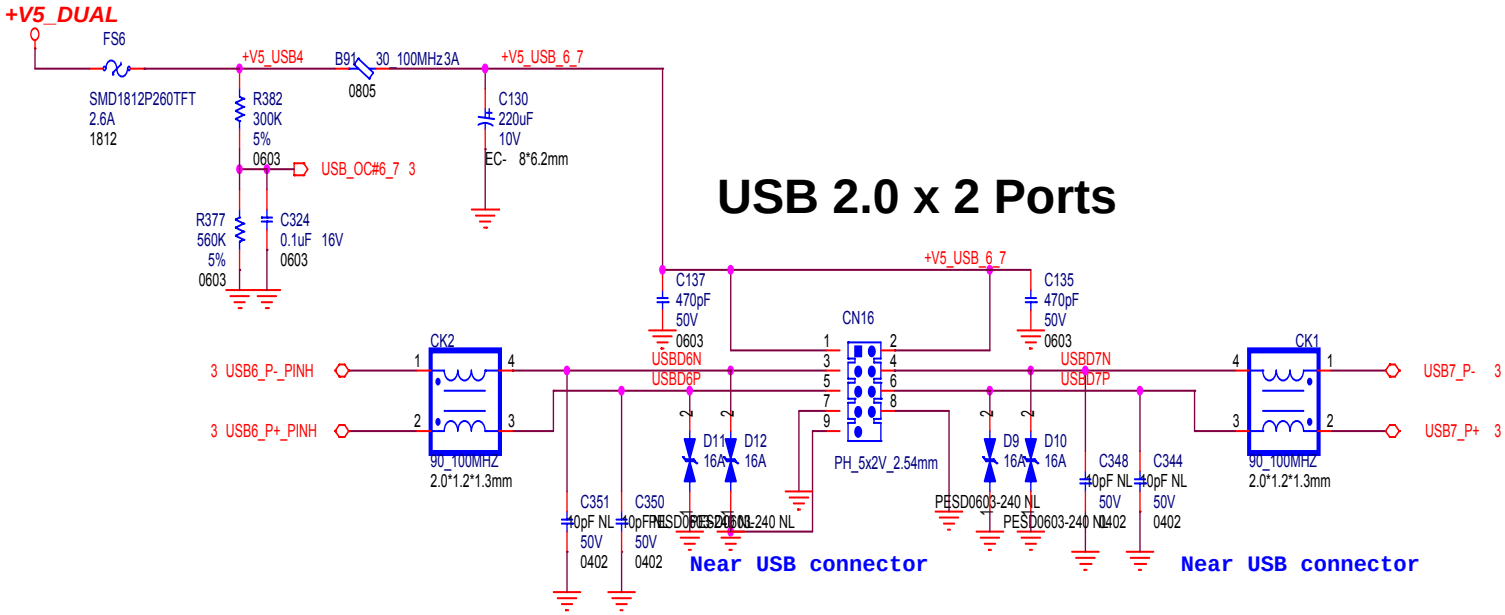


ICH8芯片 组提供HD Audio Code

USB

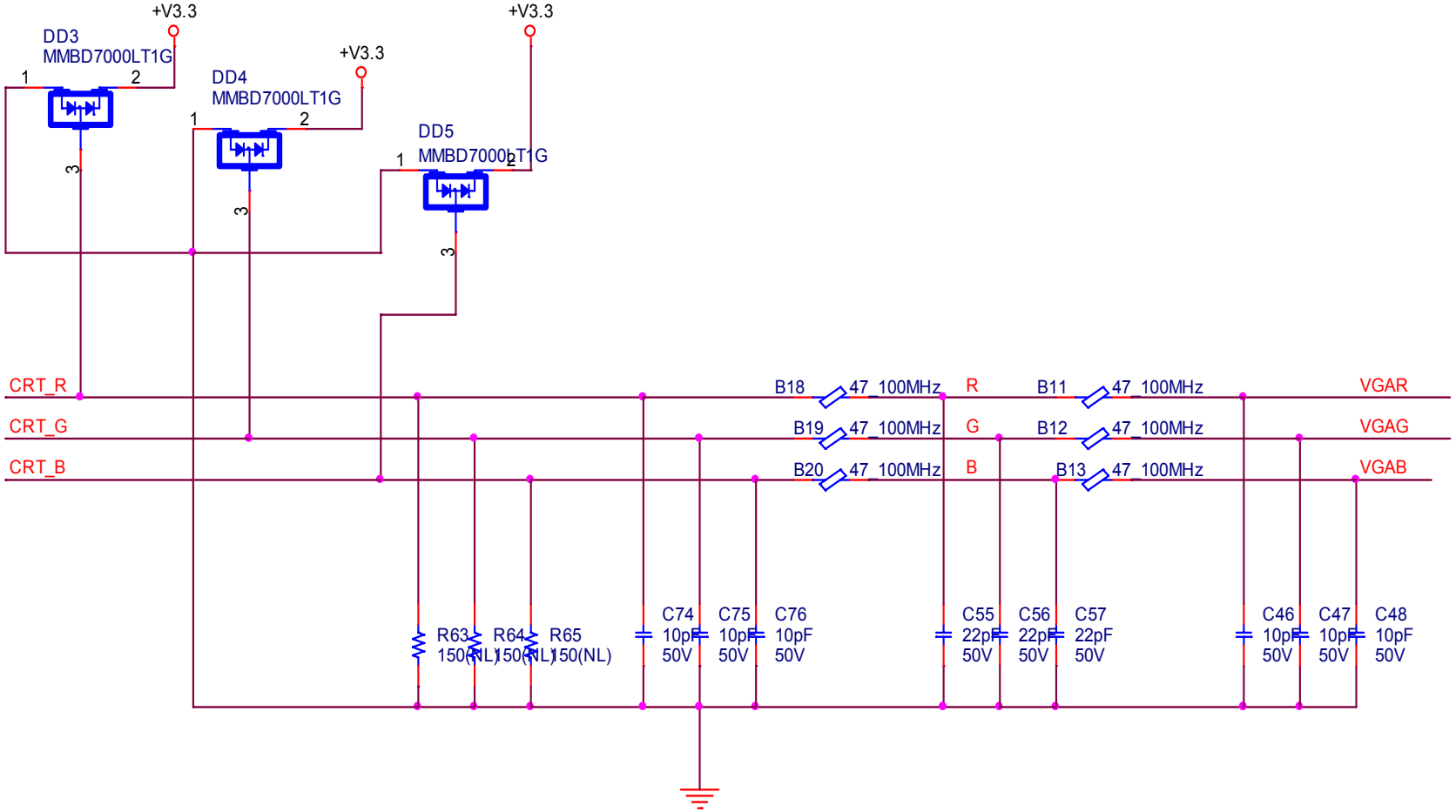
Schematic Design





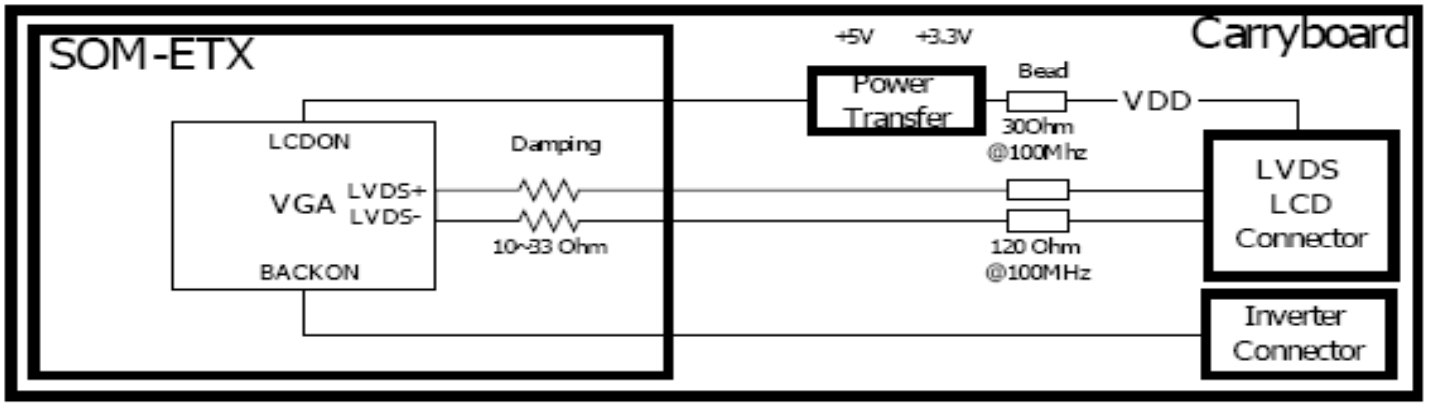
VGA

Schematic Design

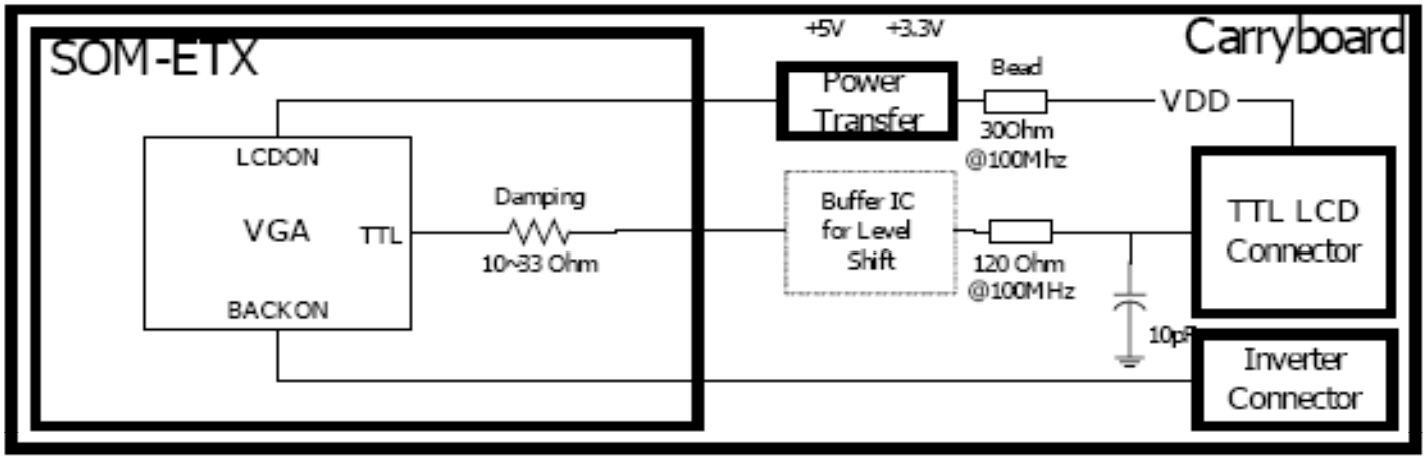


LVDS

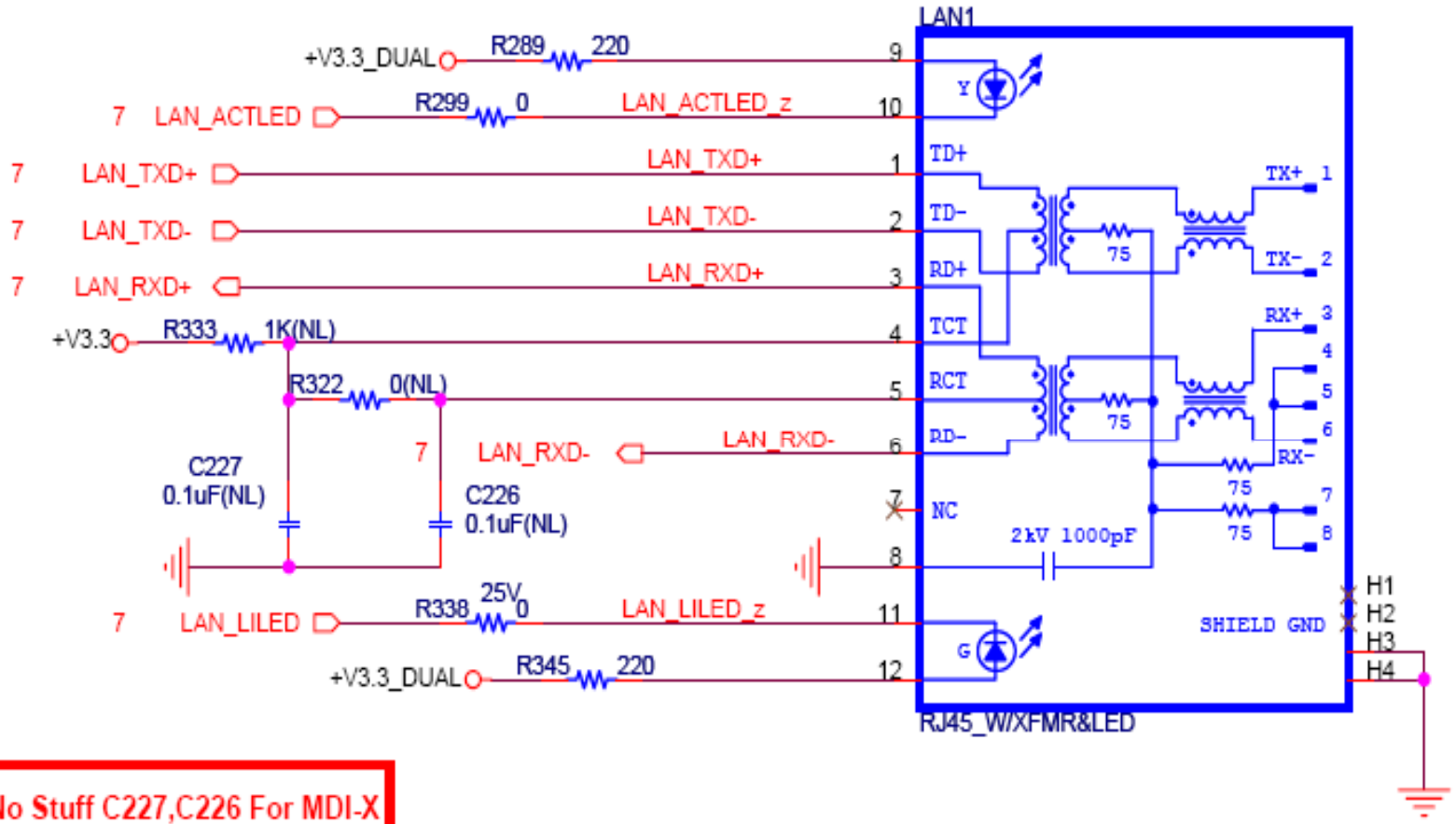
LVDS LCD Connections



TTL LCD Connections



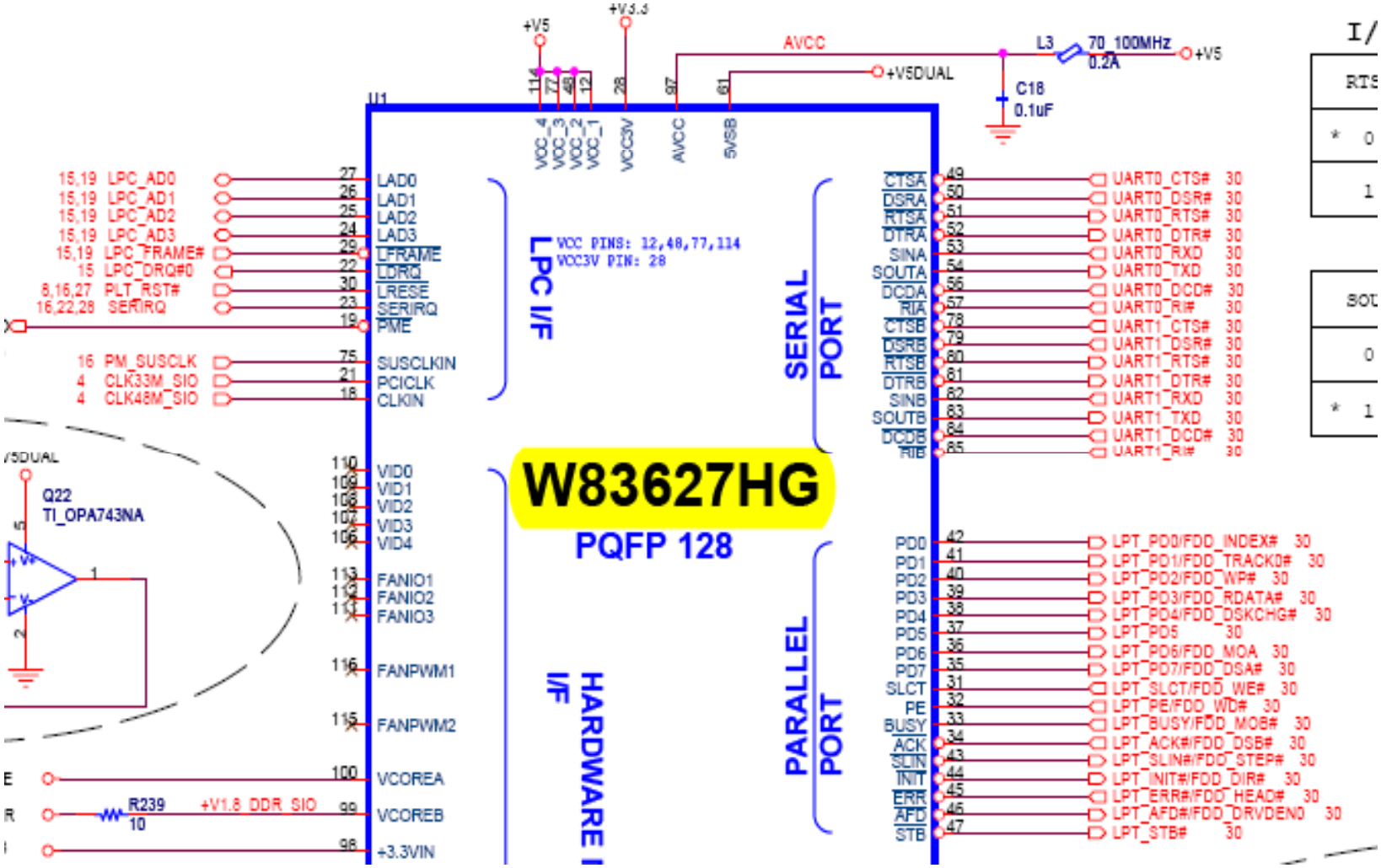
LAN



No Stuff C227,C226 For MDI-X

Only Support 10/100 LAN

Super IO Interface



SIO 芯片存在于上板，常用的IO接口直接引用即可

Power Supply

ETX™ input power sequencing requirements are as follows:

VCC_RTC **shall** come up at the same time or before VCC_5V_SBY comes up.
VCC_5V_SBY **shall** come up at the same time or before VCC_5V comes up.
PWROK **shall** be active at the same time or after VCC_5V comes up.
PWROK **shall** be inactive at the same time or before VCC_5V goes down.
VCC_5V **shall** go down at the same time or before VCC_5V_SBY goes down.
VCC_5V_SBY **shall** go down at the same time or before VCC_RTC goes down.

Figure 7-1: Power Sequencing

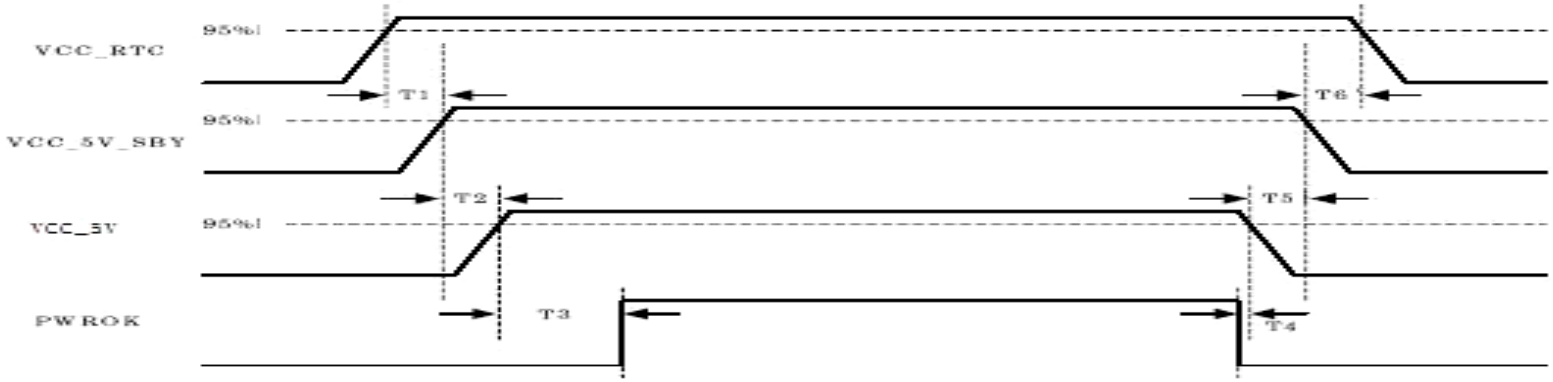


Table 7-3: Power Sequencing

T1	VCC_RTC rise to VCC_5V_SBY rise	≥ 0 ms
T2	VCC_5V_SBY rise to VCC_5V rise	≥ 0 ms
T3	VCC_5V rise to PWROK rise	≥ 0 ms
T4	PWROK fall to VCC_5V fall	≥ 0 ms
T5	VCC_5V fall to VCC_5V_SBY fall	≥ 0 ms
T6	VCC_5V_SBY fall to VCC_RTC fall	≥ 0 ms

在AT开机情况下，5VSB悬空即可

TKS